

A Proposal for Wireless Control of Submodules in Modular Multilevel Converters

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Abstract

The modular multilevel converter is one of the most preferred converters for high-power conversion applications. Wireless control of the submodules can contribute to its evolution by lowering the material and labor costs of cabling and by increasing the availability of the converter. However, wireless control leads to many challenges for the control and modulation of the converter as well as for proper low-latency high-reliability communication. This paper investigates the tolerable asynchronism between phase-shifted carriers used in modulation from a wireless control point of view and proposes a control method along with communication protocol for wireless control. The functionality of the proposed method is validated by computer simulations in steady state.

Introduction

Modular multilevel converters (MMCs) are considered as the state-of-the-art power-conversion systems for high-power conversion applications. First presented by Marquardt et al. [1], it has spread into high-voltage direct current transmission (HVDC) [2], electric railway supplies [3], and high-power motor drives [4] in recent years. The advantages of multilevel converters in general (low harmonic distortion, low dv/dt rate) and those of MMCs in specific (excellent scalability in terms of voltage and power, low switching frequency and losses, high availability due to modular structure, no need for series connection of semiconductors) make MMCs the preferred solution among voltage source converters.

MMCs may consist of hundreds of submodules. Control of the converter requires switching and sensor data exchange between a (central) controller and the submodules. Currently, this data exchange in MMCs is conducted by tethered connections, generally over optical fiber cables. However, tethered connections cause many mechanical issues in systems. Wires (especially optical fiber cables) are subject to stress and fatigue and are prone to leading a failure. Moreover, for a converter with hundreds of submodules, this cabling can be cumbersome and costly. Thus, the next step to promote the utilization of MMCs would be wireless control of submodules. The advancement can remove kilometers of cables used for control purposes, save related costs, decrease maintenance time, and increase the availability of the converter. However, this change of converter construction comes with many challenges in control and modulation of the converter since the wireless connection has fundamental differences than tethered connections in terms of latency and reliability.

The control of an MMC can be subdivided into high-level control (ac-bus and dc-bus voltage, output power), ac-bus current control, arm-balancing control (circulating current and sum capacitor voltages), modulation and submodule capacitor voltage balancing. All these control processes can be implemented either in a centralized control approach or a distributed approach. In centralized control approach, a central controller runs all the processes. It receives reference variables from higher level systems (output voltage/current, etc.), the feedback voltage and current measurements, fault and auxiliary signals from the submodules and/or other components. Then it sends tightly scheduled switching signals to the submodules for the insertion or bypass of the submodule. The communication requires high data rate and reliability but very low latency. In a

distributed approach, on the other hand, the control processes are divided between controllers in different hierarchical levels. The simplest approach for that could be to distribute the workload between the central controller and local controllers which are located in the submodules. The high-level, ac-bus current and arm-balancing controls are run on the central controller, whereas modulation and submodule capacitor voltage balancing are run on the submodules. The data exchange between the central and local controllers consists of slower dynamics such as modulation indices compared to highly deterministic switching signals in a centralized approach. Considering the stochastic nature, higher latencies and lower reliability in data transfer of wireless communication [5], a distributed control approach would be more suitable to employ than centralized approach for wireless control of submodules.

Proper modulation and capacitor voltage balancing necessitate the switching to be done in the “right” time, regardless of the modulation method. Ensuring the right timing of switching in distributed control refers to a requirement of having a common time basis for all the submodules. From the viewpoint of carrier-based modulation, which is the most generally accepted modulation method and proposed to use in this paper as well, this requirement can be expressed as the necessity of synchronized carrier waveforms in submodules. However, it is not possible to achieve a perfect synchronization between these carriers formed in different controllers because of the reasons that will be explained in the next section. Thus, this requirement forms a challenge for wireless control of submodules and the MMC should be able to function well enough with some asynchronization between these carriers. The synchronization of carriers actually depends on the synchronization of the clock sources which form the carriers in local controllers. In the literature, synchronization mechanisms for different clock sources in some distributed control approaches with tethered connections are discussed [6]-[8]. However, the amount of tolerable asynchronism between clocks and the reasoning of this amount are not clear. The tolerable asynchronism and the rate of recurrence of synchronization process are of great importance for the implementation of a wireless control method. Higher latency and lower reliability in data exchange compared to tethered communication methods are also main challenges of wireless control of submodules. Therefore, it should be avoided to rely on wireless communication for time-critical data and the data rates should be decreased. The complexity of control and excess of variables to be controlled in MMC make these requirements even more challenging.

In this paper, the effects of asynchronism between distributed clocks in submodules with respect to the harmonic quality of the ac output voltage are studied. Moreover, a control plan together with a wireless communication protocol to be used for wireless control of submodules is proposed. The study and proposal are strengthened by means of computer simulations. The paper is organized as follows: In the next section, the roots of asynchronism between carriers in local controllers are analyzed. Then, the effects of asynchronism in ac output voltage harmonic quality is investigated and a tolerable amount of asynchronism is proposed for a specific MMC configuration. Later, a wireless control method of MMC submodules is proposed along with wireless communication network and its functionality is validated by computer simulations. The conclusion is given lastly.

Analysis of Carrier Asynchronism Sources

For the modulation of MMCs, several carrier-based methods have been proposed [9]. In the distributed control approach, phase-shifted carrier (PSC) modulation is suitable and easier to implement. The carrier signal to be used in the modulation algorithm is produced by a clock source (could be an oscillator) of the submodule controller and the carrier shall be compared with the reference signal sent from the central controller or a modified version of this base signal. In the ideal case, carrier signals have exactly the required phase-shift,

$$\theta_c^k = 2\pi \frac{k-1}{N}, \quad (1)$$

where $k=1\dots N$ and N is the number of submodules per arm. This yields ideal switching-pulse patterns characterized by the reference signal. In practice, however, a clock source may deviate from its nominal frequency and have some jitter in its clock ticks. In a centralized control algorithm, since all the carriers are produced by the same central clock source, the phase-shifts are almost ideally spaced, even if the frequency of the clock source has some deviation or the clock source has a jitter in its ticks. However, in a distributed

control algorithm, there may be *secondary unintentional* phase-shifts between the carrier signals emanating from the asynchronism of the local clock sources. These secondary phase-shifts distort the ideal switching-pulse patterns, which in turn distort the ac output voltage and increase its harmonic content. The following three causes of asynchronism have been identified and their effects on carriers are illustrated in Fig.1:

1. time difference between the exact start of counting when the clock sources are powered up,
2. frequency stability and jitter of each clock source,
3. inevitable asynchronism between clock sources even after a synchronization process is performed.

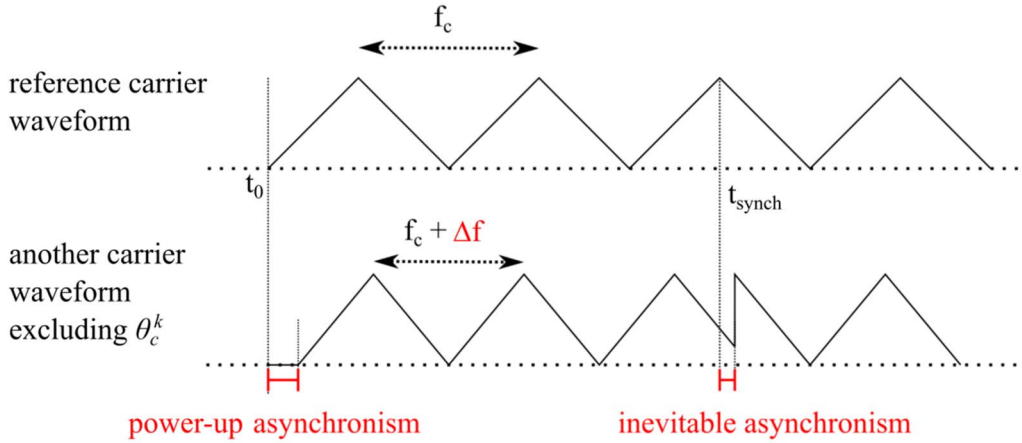


Fig. 1: Asynchronism between distributed carriers

The asynchronism emanating from the time difference between the clock's exact start of counting, the power-up asynchronism, can be regarded as temporary. It can be eliminated after the first successful clock synchronization process when the required ideal phase shifts are introduced between the carriers before the start of any modulation operation. Then, only the inevitable asynchronism is left between the carriers.

Frequency stability is related to material characteristics of the clock source and is dependent on the environmental conditions, aging, input voltage and load change of the clock source circuit component. Frequency stability of crystal oscillators is in the range of parts per million (ppm). This difference accumulates over time leading to secondary phase-shifts between carriers. Apart from frequency stability, oscillators may have jitter in their ticks which can be shortly defined as deviation of timing edges from their "ideal" locations. The jitter is grouped as deterministic and random jitter. The peak-to-peak value of deterministic jitter is finite and can be minimized by careful hardware design; however, it may still have a non-zero mean and this integrates over time causing asynchronism. On the other hand, random jitter, which is usually due to thermal noise and other uncorrelated noise sources, is considered to have a normal distribution with zero mean [10]. Having zero mean, it is reasonable to assume that random jitter does not cause asynchronism for a carrier generated by a regular sixteen bit counter.

In order to compensate for the effects of the above mentioned asynchronism causes, the clocks need to be synchronized periodically. Ideally, a synchronization process should totally eliminate time differences between clocks. In practice, there still exists some amount of asynchronism resulting from synchronization process imperfection, hardware capabilities, and measurement errors. This inevitable amount of asynchronism should be tolerable for the MMCs with regard to their low harmonic distortion of ac output voltage, which is the major advantage of multilevel converters. Together with the frequency instability and deterministic jitter of the clock source, the inevitable amount of asynchronism determines the rate of recurrence of synchronization process. In this study, the level of tolerable distortion is considered as the total harmonic distortion (THD) of line-to-neutral ac output voltage being less than 8 % taking into consideration the limit defined by [11] for converters with less than or equal to 1 kV common coupling point voltage. This value is supposed to be determined individually for each particular MMC according to its characteristics and needs. Then, the tolerable asynchronism is determined accordingly.

Realization of Asynchronism and Effects on the ac Output Voltage

The power-up asynchronism and the inevitable asynchronism can be considered as a static time difference between counters that form up the carriers and consequently as additional static phase-shifts between carriers. The frequency instability forms a dynamic source of asynchronism and it leads to increasing phase-shifts between carriers over time. It can be modeled as a disturbance in the frequency of the oscillator that drives the counter. Further, the disturbance in the oscillator frequency can be modeled as a disturbance in frequency ratio, m_f , which is defined as

$$m_f = \frac{f_c}{f_1}, \quad (2)$$

where f_c and f_1 are the frequencies of the carrier and reference (fundamental) waveforms, respectively.

In order to observe the effects of above-mentioned asynchronisms on the ac output voltage, v_s , of a PSC-modulated MMC, a series of calculations are performed by MATLAB. Calculation parameters are based on an MMC prototype. Switching-pulse patterns are obtained and the patterns are used to derive arm voltages, and ac output voltage (half of the difference of lower and upper arm voltages) of each phase leg. Thus, for this part, the resulting waveforms are normalized and idealized. They do not contain the effects of submodule capacitor voltage swing and arm impedance voltage drop. The focus of this part is to investigate the effects of asynchronism in terms of harmonic content of the converter ac output voltage. Calculation parameters are listed in Table I.

Table I: Calculation parameters

	Symbol	Value
Fundamental frequency	f_1	50 Hz
Oscillator frequency that the counters run on	f_{osc}	99.6132 MHz
Submodules per arm	N	5
Offset phase-shift amount between upper and lower arm carriers	$\delta\theta_c$	0 rad*
Number of bits of counters that form the carriers	n	16
Frequency stability of the oscillators	$\Delta f/f_{osc}$	10 ppm
Modulation index	m_a	1**

* 0 rad offset between lower arm and upper arm carriers when N is odd, results in $2N+1$ level ac output voltage and elimination of odd multiples of switching frequency harmonics pNf_c in the ac output voltage waveform [12].

** Modulation index is defined as $m_a=V_r/V_c$ where V_r and V_c are reference sinusoidal and carrier signal magnitude, respectively.

The harmonic analysis of the ac output voltage is conducted in accordance with [11]. A single measurement window width is 10 cycles. THD calculations include harmonics up to one hundredth order and an amplitude of equal to or more than 0.1 % of the fundamental. The ideal frequency ratio, m_f , is calculated as

$$m_f = \frac{f_c}{f_1} = \frac{f_{osc}/(2 * (2^n - 1))}{f_1} = 15.2. \quad (3)$$

Sinusoidal symmetric signals are used as reference voltages of the PSC modulation.

a) Ideally Phase-Shifted Carriers

Firstly, the harmonic analysis with ideal PSCs is conducted as ideal phase-shift is formulated in (1). With five submodules per arm and frequency ratio calculated in (3), the resultant ac output voltage is almost perfectly sinusoidal with zero THD.

b) Static Asynchronism in Carriers

The effects of static asynchronism that corresponds to the power-up and the inevitable asynchronisms are investigated by introducing a secondary *randomly distributed* phase-shift to each carrier. In this case, the total phase-shift is formulated as

$$\theta_c^k + \theta_j^k = 2\pi \frac{k-1}{N} + 2\pi\Delta t_k, \quad (4)$$

where θ_c^k is the ideal and θ_j^k is the secondary (unintentional) phase shifts respectively and Δt_k is random static asynchronism. The actual probabilistic distribution of the static asynchronism depends on factors related to realization and synchronization of carriers, which are not considered in this paper. However, this paper assumes that this static asynchronism has a uniform distribution. In the extreme case, the amount of secondary phase-shift is uniformly distributed within ± 1 carrier periods which, indeed, refer to no synchronization of clocks. In order to find the tolerable amount of static asynchronism, the harmonic analysis is repeated for cases with uniform distribution boundaries halved each time, i.e. $\pm 1/2$, $\pm 1/4$, and so forth.

c) Dynamic Asynchronism in Carriers

Effects of dynamic asynchronism that corresponds to the frequency instability of clock sources are studied by adding a secondary randomly distributed frequency instability term to frequency of each carrier. In this case, angular frequency of the triangular carriers is defined as

$$w_c = 2\pi(f_c + \Delta f_c) = 2\pi \left(\frac{f_{osc}}{2 * (2^n - 1)} + \frac{f_{osc} * (k * \Delta f / f_{osc})}{2 * (2^n - 1)} \right) = \frac{\pi f_{osc} (1 + k * \Delta f / f_{osc})}{2^n - 1}, \quad (5)$$

where k is a random variable. In this paper it is assumed to have normal distribution with zero mean and 1/5 standard deviation. In other words, $\Delta f / f_{osc}$, which directly effects Δf_c and is 10 ppm for our case, is assumed to have a normal distribution with zero mean and 1/5 standard deviation.

d) Combination of Static and Dynamic Asynchronism

In practice, the carriers suffer from static and dynamic asynchronism simultaneously. Thus, the harmonic analysis is conducted when carriers have the both. The carriers have a static initial asynchronism given in (4) and have a dynamic asynchronism given in (5) which integrates over time. The integration period for dynamic asynchronism is 15 consecutive 10 fundamental cycles (3 s in total), in accordance with “very short time harmonic measurements” of [11]. However, since the asynchronism terms in carriers are random variables, the resultant waveforms are not periodic and they cannot be analyzed with Fourier series expansion. They either need to be characterized over the whole ensemble of realizations or in a probabilistic framework. Both of the methods are conducted in this study as below.

The ideal ensemble of realizations consists of an infinite number of elements. For a reasonable analysis, the harmonic characterization is repeated one thousand times by introducing the asynchronism terms in carriers as independent random variables in each run. The harmonic content of the ac output voltage is root mean squared over all the runs and THD values of all the runs are shown as histograms. Calculations results when the carriers are synchronized with a tolerance of up to $\pm 1/64$ period ($\pm 20.6 \mu s$) at t_0 , and clock sources have 10 ppm frequency stability are shown in Fig. 2.

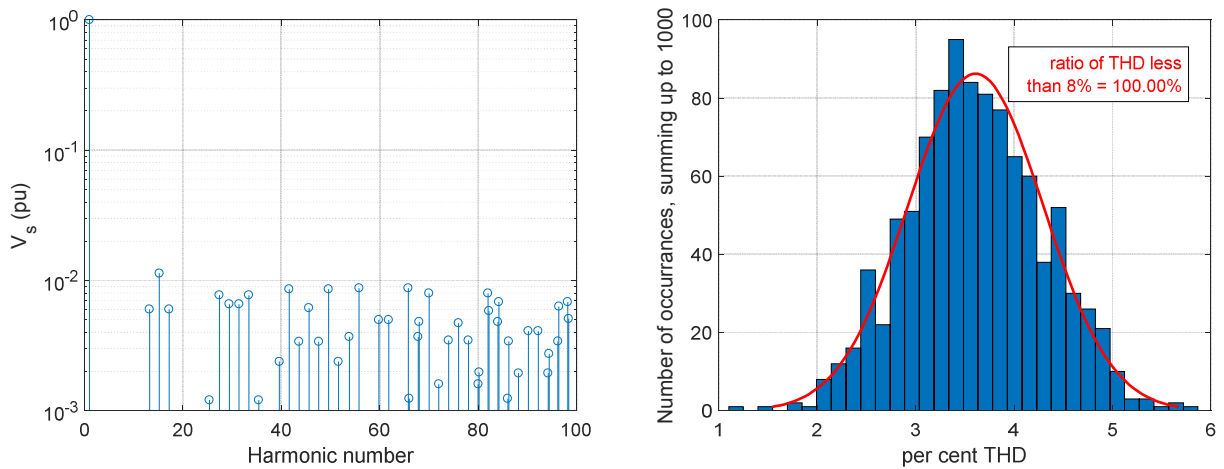


Fig. 2: Rms values of harmonics (left) and histogram of THD (right) for 15 consecutive 10 cycle windows (3 s in total) of ac output voltage, one thousand realizations in total

When ideal symmetric phase shifted carriers are used, the Fourier coefficients, C_{mn}^i , of each individual two level voltage output of a half bridge submodule can be expressed as

$$C_{mn}^i = e^{jm\left(2\pi\frac{i-1}{N}\right)} C_{mn}^1, \quad (6)$$

where C_{mn}^1 is the reference (zero phase shift) two level waveform and combinations of m and n give baseband, carrier and sideband harmonics. Moreover, the Fourier coefficients of multilevel voltage waveform sum to zero when m is not a multiple of N as expressed below

$$C_{mn} = \frac{1 - e^{jm2\pi}}{1 - e^{jm2\pi/N}} C_{mn}^1 = 0 \text{ for } 0 < m \neq pN, \quad (7)$$

where p is a positive integer. Thus the first group of voltage harmonics appear around N times the carrier frequency in ideal case, which is one of the fundamental advantages of MMCs [12]. However, as soon as the carriers have secondary unintentional phase shifts, (6) is modified with those and (7) is not valid anymore. Then, carrier and sideband harmonics start to emerge at every odd integer multiple and around every integer multiple of f_c , respectively, as can be seen in Fig. 2. The asynchronism overrules having no low frequency voltage harmonics advantage of MMCs; but the amplitudes of the emerging harmonics depend on the amount of asynchronism. For the case above, the rms values of the voltage harmonics over all realizations are less than 1 % of the fundamental except the first carrier harmonic at f_c which is still less than 2 % and is below the limit defined by [11]. Moreover, all the realizations have less than 8 % THD in their ac output voltage, again compliant with [11].

In probabilistic framework, the quantity to study a randomized waveform is the power spectrum which is the Fourier transform of the autocorrelation of the waveform. The power spectrum of a periodic function is composed of impulses at the fundamental frequency and at the harmonics frequencies with their magnitudes squared compared to the corresponding Fourier analysis components [13]. The power spectrum of a single realization of random ac output voltage is analyzed in MATLAB with Welch's power spectral density estimate and the estimate is shown in Fig. 3. It closely matches the rms values of harmonics over one thousand realizations in Fig. 2. The magnitudes of harmonics are squared in power spectral density as expected and harmonic numbers are the same.

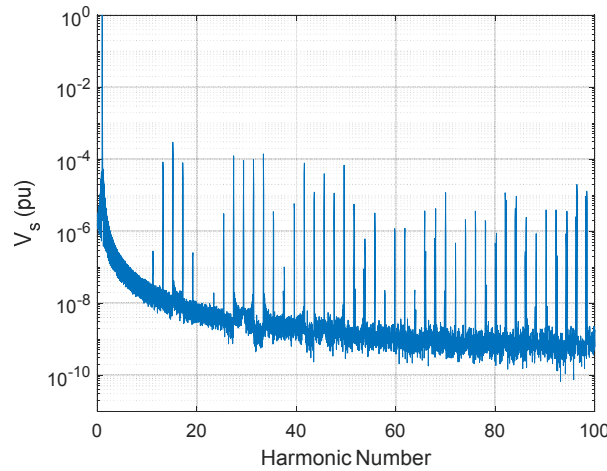


Fig. 3: Power spectral density of ac output voltage

Accordingly, the distributed clocks can be synchronized with 3 s period and $\pm 20.6 \mu\text{s}$ synchronization tolerance. Indeed, both of the figures do not put strict requirements on synchronization. However, this is an ideal modulation point of view and the rest of the circuit dynamics are excluded. A more complete view will be given in the next section. The period of synchronization can be increased either by using a more precise synchronization process (e.g. GPS clock is able to provide sub-microsecond range [14]) or more stable oscillators. It is important to note, in this analysis, the deterministic jitter of oscillators is assumed to have zero mean as the random jitter.

Proposed Control Method for Wireless Control of Submodules

Applications with time-critical control loops, like the control of MMC, require low-latency and high-reliability for the data exchange in their control algorithms. The amount of data to be transmitted is relatively low and there is no power consumption constraint. The conventional wireless systems, on the other hand, have focused on either high-throughput or low-power consumption and they are not suitable to use for such demanding applications. However, the interest on these low-latency and high-reliability communication systems has been increasing and research is ongoing in this area.

A control method which extensively utilizes time-critical signals to be exchanged between central and local controllers (e.g. switching signals) cannot be suitable for wireless control of submodules. It is convenient to use distributed control methods which permute signals that do not change in big steps instantaneously and for which the converter is robust against unsuccessful transmissions. The latency of the wireless link increases as the number of separate transmissions between central controller and local controllers increase. Thus, it is wise to decrease the number of variables and amount of data transferred over wireless link. Considering those, this paper proposes to use open-loop control of the converter [15]. The central controller is supposed to run all the required high-level control processes and generate the sinusoidal reference waveforms of modulation for each arm of the converter. These waveforms need to be transferred to the submodules over wireless link and they are not as tightly scheduled as switching pulses. PSC modulation and individual submodule capacitor voltage balancing is done in each submodule. There is no need to feed back the submodule capacitor voltages to the central controller in open loop control, which substantially relaxes the requirements on minimum data rate and latency of the wireless link. The central controller needs arm currents and ac output voltage data. Considering the total number of these feedback variables, they can be fed back with wires. Proposed control approach is shown in Fig. 4 for a phase leg of MMC and can be extended for the two other legs.

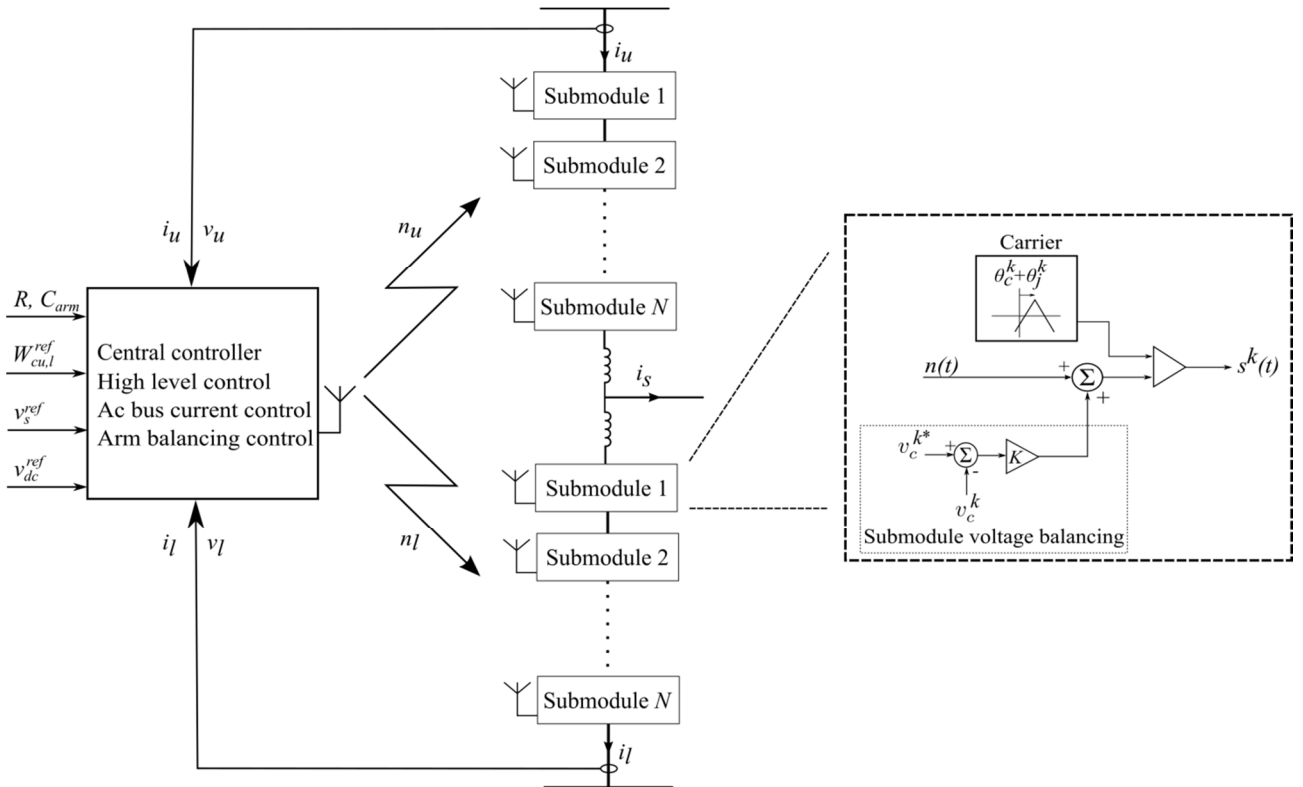


Fig. 4: Proposed control approach for wireless control of submodules of MMC

The data to be sent over wireless link, reference signals for modulation, basically consists of amplitude and phase of a sinusoidal signal. However, since the submodules receive the data packet excluding key at different time instants, there should be a time reference for the insertion indices to be updated in the modulation algorithms of the submodule controllers. Consequently, a time reference shall accompany to insertion indices. Compared to overhead of wireless data packets, total payload is small, possibly in the range of tens of bits.

Thus, it would be wise to transmit all the payloads of six arms in a single wireless data packet. Each cluster of submodules can then extract their own data from the packet. This approach enables the central controller to send updated control data for all the submodules in each consecutive transmission slot. In case some of the submodules do not receive the packet within the deadline, there is no need for re-transmission. These submodules can continue modulation with the references they have until the next reception. There will be additional, but less frequent, data transmission needs for clock synchronization (unless it is done individually in submodules through an external clock source) and in case of faults in submodules or central controller.

The wireless network proposed to be used in this paper is an Ultra-Reliable Low-Latency Communication (URLLC) protocol [16]. It is a Medium Access Control (MAC) layer protocol and transmission right is granted to the communication nodes for a limited time according to a pre-programmed plan. Reliability is increased by different transmission options including direct transmission, retransmission and relaying. In direct transmission, information is transmitted once till the end of limited access time while in retransmission mode, it is repeated twice using a weaker modulation and coding scheme. In relaying, data is transmitted via a relay (an additional node) to the receiver(s) so that cooperative diversity is exploited and indeed principally relaying enables the protocol to have low-latency and high reliability. This MAC layer protocol is implemented on top of IEEE 802.11a/n [17] physical layer (PHY).

The functionality of the proposed control method is validated by simulating a three phase MMC in MATLAB Simulink in inverter mode of operation. In addition to those given in Table I, simulation parameters are given in Table II.

Table II: Simulation parameters

	Symbol	Value
Dc link voltage	V_{dc}	500 V
Load resistance	R_o	8.84 Ω
Submodule capacitance	C	2.7 mF
Arm inductance	L_{arm}	5 mH
Arm parasitic resistance	R_{arm}	0.01 Ω
Synchronization period of carriers in submodules	-	100 ms
Synchronization tolerance of carriers in submodules	-	$\pm 1/64$ period ($\pm 20.6 \mu\text{s}$)

In order to mimic the wireless link, each wireless transmission slot is taken as 100 μs including total payload to the six arms, MAC and PHY overhead. Reference waveform from the central controller is sampled with 100 μs period. Then the sample is sent to submodules with independent random latencies with half-normal (one-sided normal) distribution and 25 μs standard deviation. Hence, 99.9936 % of the data is assumed to be received by the submodules within four standard deviations, 100 μs , and corresponding packet error rate (PER) is $6.33 \cdot 10^{-5}$. The carriers in the submodules are synchronized according to the figures in the table assuming uniform distribution in synchronization tolerance as proposed previously. The synchronization period was allowed to increase up to 3 s from solely output harmonic quality point of view. However, the capacitor voltage balancing and circulating current suppression requires more frequent carrier synchronization. Due to random variables both in the carrier waveforms and latencies in the reference data transmission link, the simulation is run one hundred times to deduce reasonable results and rms values of resultant signals over all the realizations are calculated. The graphs in Fig. 5 show the results.

According to the graphs, output voltage has low frequency odd harmonics well below 1 % of fundamental and the biggest harmonics are at the sidebands of $N \cdot f_c$ with and amplitudes around 1 % of fundamental. THD of voltage harmonic, 1.83 %, is well below the limits of [11]. The current harmonics are the 5th harmonic, at the first carrier harmonic and the 5th sidebands of $N \cdot f_c$. Individual capacitor voltages are a bit spread with respect to each other in 3-4 V range, but the voltage spread reached a steady state and sum capacitor voltages are very close to each other. Ac component of circulating current is around 5 % of its rms value with majority of the dominant harmonics being at the sidebands of $N \cdot f_c$ (not shown here). Considering the results, it can be argued that the submodules of MMC can be controlled wireless with the proposed control method and communication protocol in steady state.

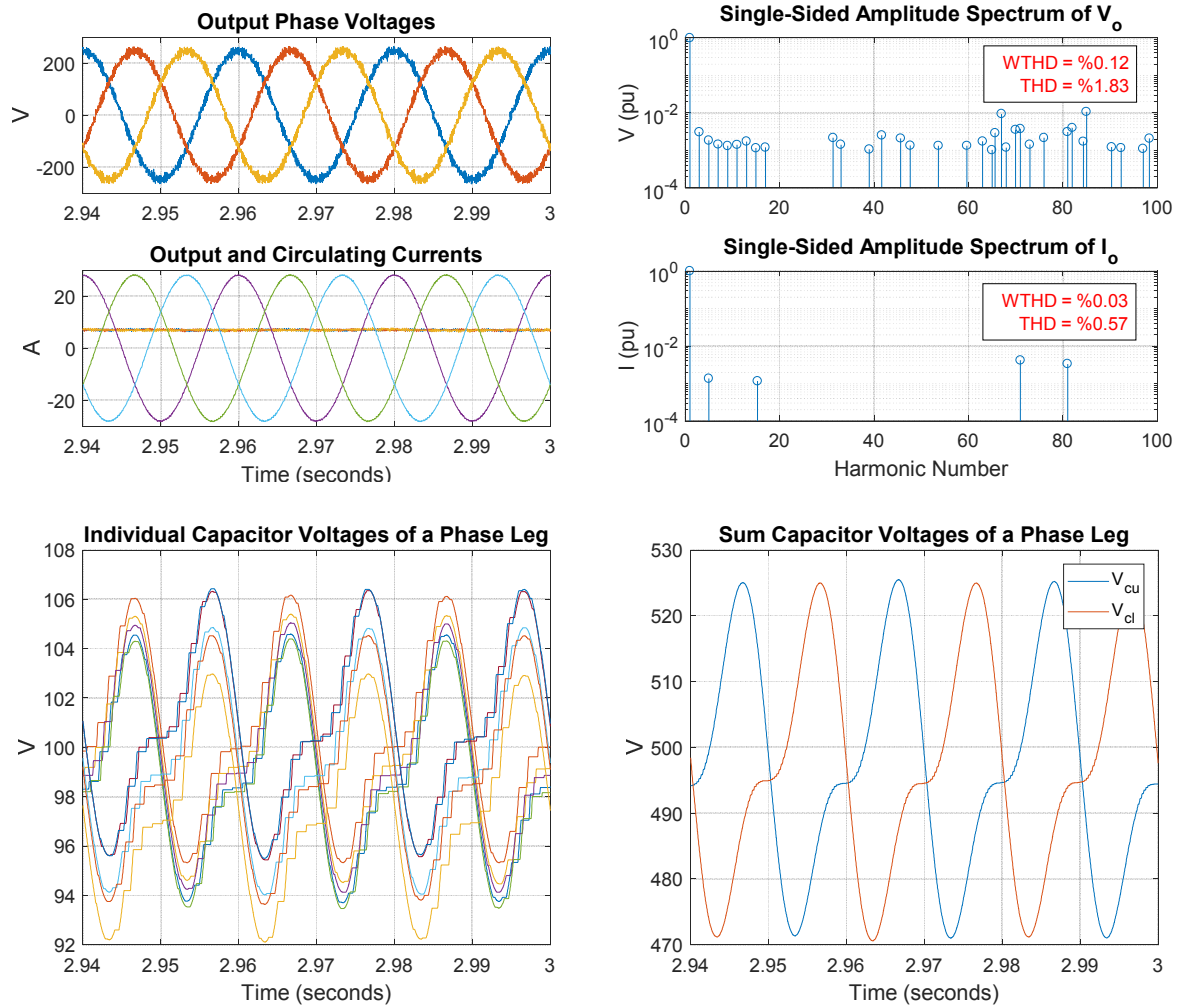


Fig. 5: MMC output phase voltages, output and circulating currents (top left), output phase voltage and current harmonic spectrums (top right), individual capacitor voltages of a phase leg (bottom left) and sum capacitor voltages of a phase leg (bottom right)

Conclusion

Wireless control of the submodules would be the next advancement in the evolution of the MMCs, as being an alternative for the cumbersome and costly cables going to hundreds of submodules. However, this change of converter construction comes with many challenges in control and modulation. In this paper, the tolerable asynchronism amount between distributed PSCs in submodules is investigated in terms of converter ac voltage harmonic quality. The amount of tolerable asynchronism shall be considered individually for each different system using the methodology defined. For a sample MMC with five submodules per arm, it is shown that the tolerable asynchronism amount is approximately $\pm 1/64$ period of carriers ($\pm 20.6 \mu\text{s}$) when m_f is 15.2. Moreover, a distributed control and modulation approach and the communication protocol are proposed for wireless control of submodules. The functionality of the proposed method is validated by computer simulations taking into account the possible challenges like asynchronism between carriers and latency in wireless communication. However, more work needs to be carried over to investigate the proposed control method for a bigger MMC with tens/hundreds of submodules per arm. For sure, the proposal needs to be validated by showing its operability in an experimental setup and the work should be extended for fault cases in submodules, central controller and data transmission.

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