Wireless control of modular multilevel converter autonomous submodules

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Abstract

The wireless control of modular multilevel converter (MMC) submodules might offer advantages for MMCs with a high number of submodules. However, the control system should tolerate the stochastic nature of the wireless communication, continue the operation flawlessly or, at least, avoid overcurrents, overvoltages, and component failures. The previously proposed control methods enabled to control the submodules wirelessly with consecutive communication errors up to hundreds of control cycles. The submodule control method in this paper facilitates the MMC to safely overcome communication errors that last longer and when the MMC experiences significant electrical disturbances during the errors. The submodules are proposed to operate autonomously by implementing a replica of the central controller in the submodules and drive the replicas based on the local variables and the previously received data. The simulation and experimental results verify the proposed control method.

Introduction

The modular multilevel converter (MMC) is the prominently used voltage-source converter for high-voltage dc (HVDC) transmission systems. Scalability of the power and voltage ratings using off-the-shelf power semiconductors and low harmonic distortion are two features that favor MMCs for HVDC transmission. Obtaining high voltage and power ratings for the converter necessitates employing a high number of submodules, which also contributes to having low harmonic distortion, but results in a costly communication system between the controller(s) and the submodules. Wireless control of MMC submodules, which has been proposed in [1], implemented, and verified in [2], might be helpful to reduce the communication system cost. Optical-fiber links are the most used communication medium in MMCs [3, 4]. The layout of the fiber cables in the converter hall is time-consuming and prone to errors. Consequently, wireless control of submodules might shorten the converter installation time and increase the availability of the converter. On the other hand, wireless communication introduces stochasticity and anomalies in the control system. The wirelessly transmitted data might be lost or delayed [5]. Thus, the overall MMC control system should tolerate losses and delays in the data transmission to some extent and continue the operation flawlessly. If the errors in the data transmission become extraordinarily long, then the controller should be able to keep the converter operation within safe limits and protect the converter components from failures.

Wireless control in [1, 2] is based on a distributed MMC control approach. In distributed control, the submodules have their controllers onboard conducting the *switching control* duties, i.e., carrier-based modulation and submodule capacitor voltage control. The central controller conducts the *converter control* duties, which include the ac-side current control, arm balancing control, and circulating current control

[6]. The central controller generates the insertion indices of each phase arm of the MMC. Consequently, the fundamental wireless data to transmit from the central controller to the submodules are the insertion indices and the synchronization signal for the modulation carriers in the submodules. The random delays in the wirelessly transmitted data are minimized by the concordantly working control and communication systems in [2]. Wireless data packet losses up to a few consecutive control cycles are treated by decreasing the closed-loop system control bandwidth. In [7], submodule controllers are proposed to have a set of resonant filters to locally extrapolate the previously received insertion indices in case of experiencing wireless packet loss trains. The extrapolated indices follow the pre-packet-loss pattern. In this sense, a sort of *open-loop* control is provided during the loss period. This control method performs satisfactorily for a limited interval, possibly up to hundreds of control cycles [7]. However, in the case of loss trains with extreme length, i.e., more than hundreds of control cycles, there are two possible problems if this open-loop control continues. Firstly, the locally extrapolated insertion indices might become obsolete due to changes in the control system references, converter state variables, or disturbances on the ac or dc-sides. The continued control of the submodule(s) with such an open-loop control might lead to off-reference output current/power, overcurrents, overvoltages, and the loss of stability. Moreover, during the packet-loss period, the phase-shifts of the modulation carriers in the submodules deviate from their ideal values, and the deviation accumulates with time [1]. The result is erroneous modulation which ends up as over/undervoltages in the submodule capacitors and distortion on the ac-side variables, and similar issues above.

In this paper, in case of extremely long packet losses, the submodules that suffer from the wireless packet losses are proposed to switch from the open-loop control method to a locally operated *closed-loop* control. The local controller works *autonomously* with the measured/estimated variables in the submodule and the previously received data. Using the local controller, the submodule(s) experiencing packet loss can continue the operation within safe limits. The submodule(s) remains in autonomous operation until the wireless communication is recovered. Then, it switches back to the control with insertion indices transmitted from the central controller.

Autonomous Operation of MMC Submodules

In the distributed control applications of the MMC, apart from the central controller, the submodule controllers take part in the overall MMC control system. The central controller and the submodule controllers work in a master/slave fashion. The share of the MMC control algorithms between the central controller and the submodule controllers varies in different implementations of the distributed control. The submodules are responsible for modulation and submodule capacitor voltage control in the most prominent distributed control implementation [1, 2, 8, 9]. In other examples, on top of these two tasks, the submodule controllers are involved in the ac-side current control of the MMC [10, 11]. This paper principally proposes to combine the former and a modified form of the latter implementation for the wireless control of the submodules and use these methods in turn depending on the wireless communication status of the submodules. The resultant control system provides autonomy to the submodules, which is required to compensate for the wireless communication errors. (Autonomous control systems are defined to compensate for significant failures in the plant and the environment without external intervention [12].) The proposed operational modes for a wirelessly controlled submodule are:

1. Mode 1 (M1): As long as the submodule receives wireless data from the central controller, it conducts the modulation and submodule capacitor voltage control based on the received insertion indices. This mode of operation corresponds to the distributed control method given in [1, 2, 8, 9]. If the submodule experiences a single packet loss, it uses the previously received insertion index for the next control cycle.
2. Mode 2 (M2): If the submodule experiences two-cycle or longer packet losses (loss train), the submodule extrapolates the previously received insertion index and continues modulation unless the loss train is longer than a predefined safe-operation interval or the measured/estimated local variables, e.g., submodule capacitor voltage, exceed the safety limits. This mode of operation corresponds to the control method proposed in [7].

3. Mode 3 (M3): In case of excessive loss trains longer than the predefined interval for M2, or if any of the measured/estimated local variables exceeds the safety limits during M2, the submodule switches to the autonomous operation and runs with the local controller. This mode of operation resembles the control method in [10, 11], but with the critical difference, the controller in this mode needs to operate with the locally measured, calculated, or previously received variables and references.
4. Mode 1 (M1): When the submodule receives wireless data from the central controller again, while it is in M2 or M3, it switches back to the regular distributed control in M1.

Submodule Closed-Loop Current Controller Design

The current controller in the submodules is proposed to replicate the ac-side current controller in the central controller. The ac-side current controller in the central controller and its replicas in the submodules should ideally produce the same ac-side voltage reference $v_s^\star$ if they have the same input variables and controller parameters. When the communication is lost in the submodules, if the input variables to the controllers in the submodules remain close to those in the central controller, then the closed-loop control can be sustained locally using the indices generated onboard. During the regular operation, i.e., in M1, the central controller can share the input variables of the ac-side current controller with the submodules. However, in the case of long packet losses after the above-defined M2, and indeed when needed, the inputs of the controller should either be measured, calculated, or assumed/defined locally.

In this paper, a single-phase MMC with a proportional-resonant (PR) ac-side current controller is investigated. The same concept applies to three-phase MMCs with PR controllers. Then, the controllers in the submodules are also PR type. It is favorable to have PR controllers in the submodules as they do not require the point of common coupling (PCC) voltage angle as in proportional-integral (PI) controllers, which would sharpen the control complexity with the loss of wireless data. It is hypothesized that the concept can be extended to three-phase MMCs with PI controllers in the central controller but PR in the submodules.

The transfer function of the PR current controller for the fundamental angular frequency ω_1 is given as

$$G_{\mathrm{PR}}(s) = K_P + K_1 \frac{s\cos\phi_1 - \omega_1 \sin\phi_1}{s^2 + \omega_1^2}, \tag{1}$$

where s is the complex Laplace variable, K_P is the proportional gain, K_1 is the resonant gain, and ϕ_1 is the compensation angle for the total time delay. The block diagram of the ac-side current control loop is shown in Fig. 1, where v_a is the PCC voltage, v_a^f is the PCC voltage feedforward, and $G_p(s)$ is the plant transfer function.

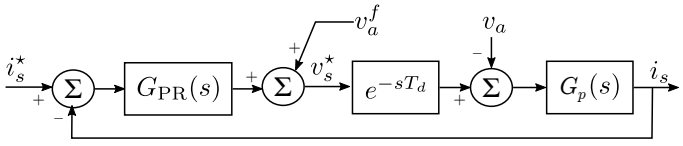

Fig. 1: Ac-side current control loop.

In M1, the central controller can share the inputs to the controller, $i_s^\star$, i_s, and v_a^f, with the submodules along with the same data package that conveys the insertion indices of the submodules. The submodule controllers receive these variables with the wireless communication delay, which should be taken into account when the variables are to be used in the controller. In this paper, v_a^f is discarded in the submodule controllers to simplify the design. Regarding i_s, it should be obtained locally when the controller replica in the submodule takes over the control in M3. One straightforward way is to have a current sensor(s) on the submodule terminals, measure the upper or lower arm current, i_u or i_l, by

$$i_u = \frac{i_s}{2} + i_c \qquad i_l = -\frac{i_s}{2} + i_c \tag{2}$$

where i_c is the circulating current, which ideally is dc. A moving-average filter (MAF) can be used to remove i_c and derive i_s from (2). Although straightforward, this method requires current sensors in the submodules, which may not be preferred due to their cost and negative impact on reliability. Alternatively, $i_{u/l}$ can be obtained from the submodule capacitor charging dynamics. If the submodule is inserted in the current path, $i_{u/l}$ can be obtained from

$$i_{u/l} = C\frac{dv^i_{cu/l}}{dt}, \tag{3}$$

where C is the submodule capacitance and $v^i_{cu/l}$ is the submodule capacitor voltage. As the submodule is continuously inserted in and bypassed out from the current path, (3) should run in the submodule controllers only when the submodule is inserted, and the resultant current should be low pass filtered with a high bandwidth filter. (The attenuation and phase-shift introduced by filtering can be compensated.) The filtered current, $\overline{i_{u/l}}$, can be used to derive i_s using an MAF. Deriving an accurate arm current depends on knowing the submodule capacitance value accurately. Thus, the capacitance value should be periodically updated with a proper method during normal operation [13]. Moreover, the capacitor voltage measurement circuit should have a sufficiently high precision to calculate the derivative of the voltage between the consecutive control cycles. The period of control cycles might be in the order of tens of microseconds.

From the submodule perspective, there is no obvious way to obtain $i_s^\star$ on-the-fly when there is no communication from the central controller. Then it can either be extrapolated according to the previously received data and/or converged to a safety-oriented value, possibly to zero. With the open-loop control in M2, the submodule is operated with an intrinsically extrapolated $i_s^\star$ by extrapolating the insertion indices. Then it is considered safer for the submodule and the converter not to continue the control with an already outdated $i_s^\star$ from the operational point of view. Therefore, $i_s^\star$ is proposed to ramp down to zero in M3. It should be considered that during the packet loss interval, the modulation carriers in the submodules drift away from their ideal phase-shifts due to lack of synchronization, which ends up as a divergence of capacitor voltages from their ideal value [1]. The rate of divergence is proportional to i_c and i_s [14]. Hence, it is reasonable to ramp down $i_s^\star$ for this reason as well. In order to have a smooth ramp-down period in M3, $i_s^\star$ in the submodule controllers should have a similar magnitude and phase to its counterpart in the central controller when starting the ramp-down period. This similarity can be realized by extrapolating $i_s^\star$ throughout M2 and during the ramp-down period of M3. The extrapolation of $i_s^\star$ is realized by a zero-bandwidth resonant filter, which is obtained from its general form

$$H_h(s) = \frac{K_h(s\cos\phi_h - h\omega_1\sin\phi_h)}{s^2 + \alpha_h s + (h\omega_1)^2}, \tag{4}$$

by setting h to 1, ϕ_h and α_h to 0. The resonant filter should have negative feedback from its output and K_h should be set to 0 for $i_s^\star$ extrapolation during packet losses. Moreover, as mentioned above, there is a phase-shift between the $i_s^\star$ in the central controller and that received in the submodule controllers due to the time delay originating from the wireless communication. If the delay is approximately fixed as in [2], it can be compensated in the submodules using a resonant filter as in (4) and setting ϕ_h to the phase-shift corresponding to the delay. Then $i_s^\star$ in the central and submodule controllers are almost in-phase. When packet loss train occurs, and the submodule switches to autonomous operation after the predefined interval in M2, the extrapolated and phase-corrected $i_s^\star$ can be ramped down to zero with a predefined slope. The block diagram of the autonomous controller for a lower arm submodule is shown in Fig. 2, where $v_c^\star$ is the internal voltage reference and v_{cl}^Σ is the lower arm sum capacitor voltage. The insertion indices can be synthesized in the submodules with the direct voltage control (direct modulation) method and without circulating current control [17]. Hence, $v_c^\star$ is taken as $V_{\mathrm{dc}}/2$ and v_{cl}^Σ as V_{dc}.

Transitions Between the Control Modes

The transitions from one control mode to another are particular instants for the operation of the submodules. They might end up in steep insertion index changes, which can lead to overcurrents in the arm and

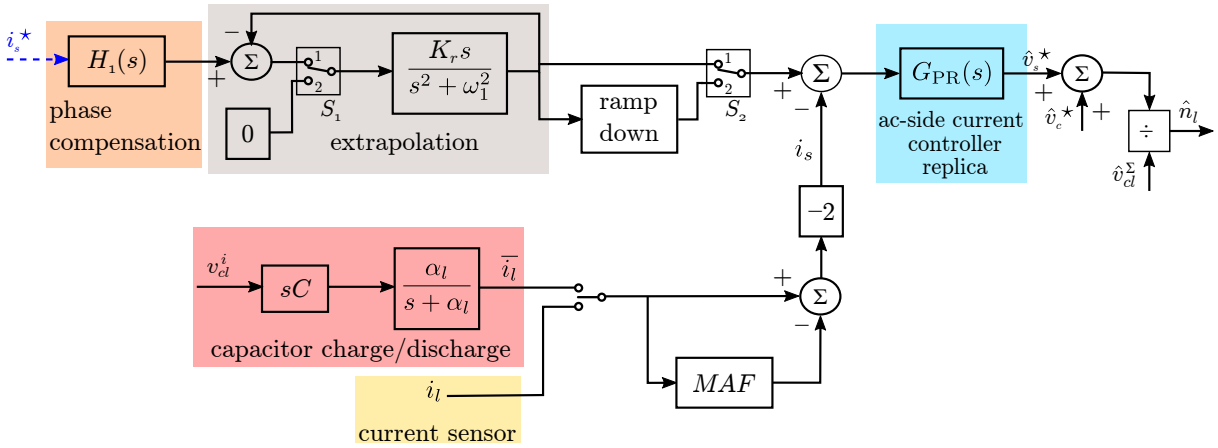

Fig. 2: Autonomous lower arm submodule controller. $i_s^\star$ is wirelessly received. S_1 switches to position 2 in M2 and M3. S_2 switches to position 2 in M3. i_s is obtained either by submodule capacitor charging dynamics or by the local current sensor if it exists.

ac-side currents and over-voltage in the submodule capacitors when the MMC is connected to an active load. The transition from M1 to M2 is smooth as the same insertion index pattern is continued within the packet loss interval [7]. The transition from M2 to M3 is an open-loop to closed-loop control change. The lack of a feedforward term in the submodule controllers, the increase of the resonant controller output in M2 due to open-loop operation, variations in the communication delay, filtering effects, and other non-idealities cause the submodule controller to have a significantly different insertion index at the transition instant than the extrapolated index at the end of M2. Similarly, the transition from M3 to M1 is from the local closed-loop control to the central closed-loop control, and it is possible to experience steep changes in the insertion index, especially if $i_s^\star$ is ramped down to zero in M3. The effects increase as more submodules experience the mode transitions. Hence, to avoid such issues, instead of changing the operational mode instantly, the transitions are extended over a fixed time interval in which the insertion indices from the pre-transition and post-transition modes are combined. The weight of the pre-transition mode insertion index is decreased by time from 100 % to 0 %, and the post-transition mode insertion index is increased oppositely. Moreover, the input to the resonant controller in the central controller is zeroed to avoid wind up if the ac-side current is less than 80 % of its reference value.

Wireless Control with Autonomous MMC Submodules

The proposed wireless control method with autonomous MMC submodules is simulated in MATLAB-Simulink and experimented with using a single-phase laboratory-scale MMC consisting of half-bridge submodules and working in rectifier mode. The simulated and experimented circuit diagram is shown in Fig. 3 left, and the experimental setup in Fig. 3 right. The MMC is connected on the ac-side to a two-level voltage-source converter over a *CL* filter, which practically forms an *LCL* filter with the arm inductors, and on the dc-side to a direct voltage source in parallel with a resistive load. A phase-locked loop (PLL) based on inverse Park transform is used for synchronization with the converter on the ac-side [15]. The MMC parameters are given in Table I. PR controllers are used for the ac-side current and circulating current control. The open-loop voltage control method is used for the arm-balancing control [16]. Phase-shifted carrier-based modulation and individual submodule-capacitor-voltage control are employed in the submodules. The carriers are synchronized periodically. Controller parameters are given in Table II. They are chosen according to the controller design suggestions in [17]; the process is not repeated for brevity. The ac-side current controller block diagram is shown in Fig. 4.

The open-loop transfer function from the grid current error i_e to measured grid current i_g is obtained as

$$\frac{i_g(s)}{i_e(s)} = G_{\mathrm{kc}}(s) = \frac{G_{\mathrm{PR}}(s)e^{-sT_d}(sC_fR_d+1)}{s^3C_fL_cL_f + s^2[C_fL_fG_{\mathrm{PR}}e^{-sT_d} + C_fR_d(L_f+L_c)] + s(L_f+L_c)}, \tag{5}$$

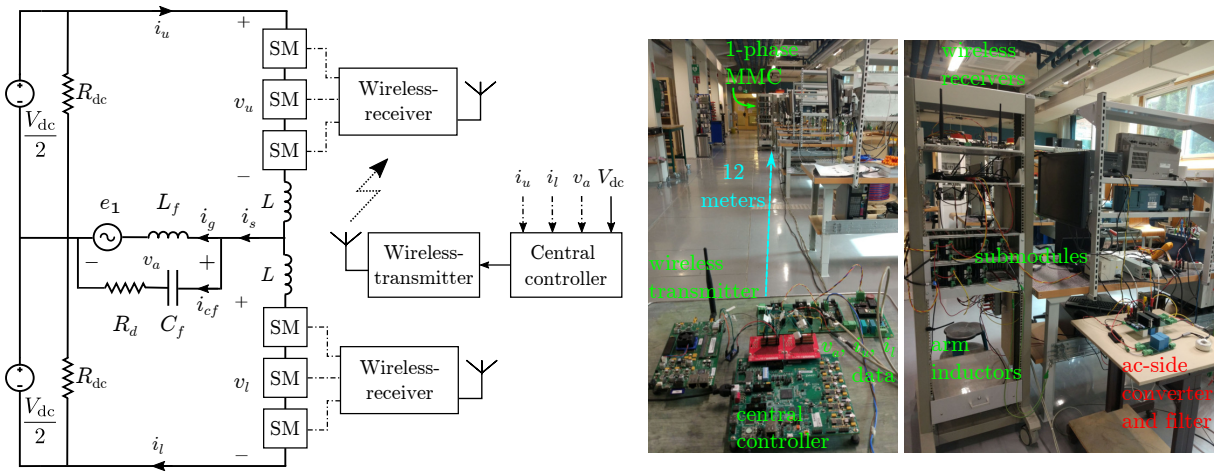

Fig. 3: Simulation and experimental study circuit diagram (left) and experimental setup (right).

Table I: MMC parameters

	Symbol	Value		Symbol	Value
Fundamental frequency	ω_1	$2\pi 50$ rad/s	Arm parasitic resistance	R	0.3 Ω
Modulation carrier frequency	f_c	833 Hz	Arm inductance	L	3 mH
Submodules per arm	N	3	Submodule capacitance	C	2.7 mF
Dc-side voltage	$V_{\rm dc}$	84 V	Filter inductance	L_f	76 μH
Dc-side resistor	$R_{\rm dc}$	10 Ω	Filter capacitance	C_f	30 μF
Ac-side source peak voltage	$\hat{e}_1$	40 V	Filter damping resistor	R_d	2.3 Ω

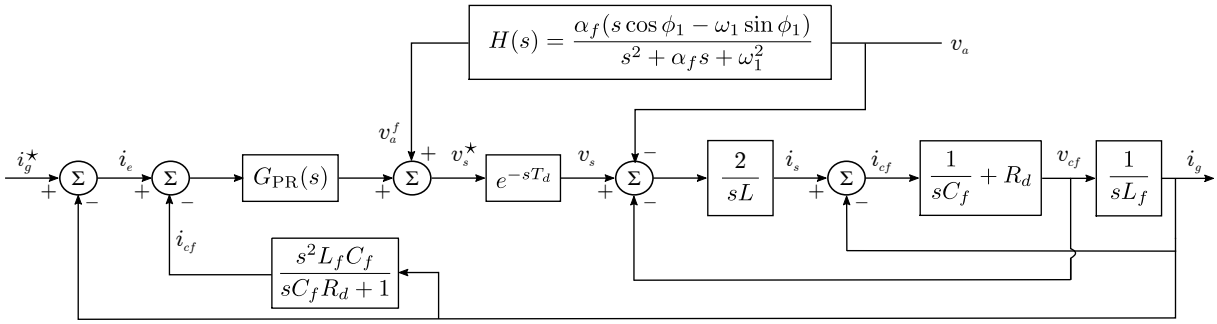

Fig. 4: The block diagram of the ac-side current control loop for the central controller.

where L_c is equal to $L/2$ and R is ignored. The ac-side admittance of the MMC is obtained as [18]

$$Y_c(s) = \frac{2[1 - e^{-sT_d}H(s)]}{(sL+R)[1+G_{\rm kc}(s)]}, \tag{6}$$

where $H(s)$ is the bandpass filter of PCC voltage feedforward as given in Fig. 4. The Nyquist plot of $G_{\rm kc}(s)$ and the real part of $Y_c(j\omega)$ are given in Fig. 5 left. The ac-side current closed-loop system is stable with a 63° phase margin. $Re\{Y_c(j\omega)\}$ becomes negative in the vicinity of ω_1, which is due to having PCC voltage feedforward and resonant controller together, and from $25\omega_1$ onward, due to the time delay. The circulating current controller block diagram is the same as in [2, Fig. 6]. The circulating current closed-loop system is stable with a 49° phase margin.

The stability of the closed-loop system using local controllers is analyzed for the case i_s measured with current sensors. Excluding the *CF* filter, the open-loop transfer function and the ac-side admittance

Table II: Controller parameters

	Symbol	Value
Central controller sampling frequency	ω_s	$2\pi 10$ krad/s
Ac-side-current reference peak value	$\hat{i}_s^\star$	4 A
Ac-side-current controller closed-loop-system bandwidth	α_c	$\omega_s/60$ [rad/s]
Ac-side-current controller proportional gain	K_p	$\alpha_c(L/2+L_f)$ [Ω]
Ac-side-current resonant controller bandwidth	α_1	$\alpha_c/10$ [rad/s]
Ac-side-current controller resonant gain	K_1	$2\alpha_1 K_p$ [Ω/s]
Circulating-current controller virtual resistance	R_a	$\alpha_c L/2$ [Ω]
Circulating-current resonant controller bandwidth	α_2	50 rad/s
Circulating-current controller resonant gain	K_2	100 Ω/s
Autonomous submodule cont. low pass filter bandwidth	α_l	$100\omega_1$ [rad/s]
Autonomous submodule cont. resonant filter gain	K_r	100 Ω /s
PLL closed-loop-system bandwidth	α_p	$\alpha_c/10$ [rad/s]
PLL integral-part bandwidth	α_{ip}	$\alpha_p/10$ [rad/s]
Total time delay from the central controller to the submodules [2]	T_d	242 μs

resulting from the submodule controllers are

$$G_{\mathrm{ks}}(s) = \frac{2\{G_{\mathrm{PR}}(s)e^{-sT_d}[1-G_{\mathrm{MAF}}(s)]\}}{sL+R}, \qquad Y_s(s) = \frac{2}{(sL+R)[1+G_{\mathrm{ks}}(s)]}, \tag{7}$$

where $G_{\mathrm{MAF}}(s)$ is the transfer function of the MAF with 20 ms window length. The Nyquist plot of $G_{\mathrm{ks}}(s)$ and the real part of $Y_s(j\omega)$ are given in Fig. 5 right. The ac-side current closed-loop system is stable with an 84° phase margin. $Re\{Y_s(j\omega)\}$ is non-negative up to $\omega_s/2$.

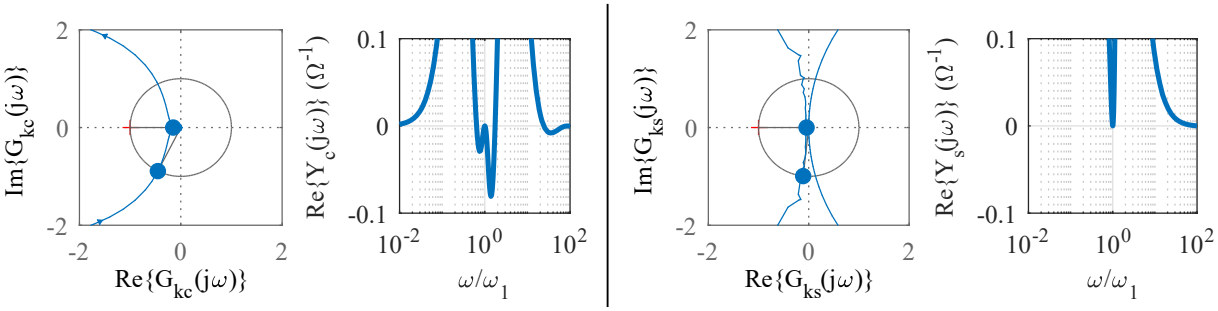

Fig. 5: Nyquist plot of $G_{\mathrm{kc}}(s)$ and the real part of $Y_c(j\omega)$ (left) and Nyquist plot of $G_{\mathrm{ks}}(s)$ and the real part of $Y_s(j\omega)$ (right).

In the simulation and the experiment, the maximum operation time in M2 is defined as two fundamental cycles, i.e., 40 ms. The operational mode transitions from M2 to M3 and from M3 to M1, and also the $i_s^\star$ ramp-down interval at the beginning of M3 are held in 84 ms each. The ac-side current in the submodules is obtained by the submodule capacitor charging dynamics during M3 in the simulation work. In the experimental work, the measured ac-side current is used in the submodules during M3.

Simulation Study and Discussion

The proposed control method is benchmarked against the existing control methods in [2] and [7]. The simulated circuit diagram is shown in Fig. 3, left. During the regular operation, the submodules have a packet loss ratio of 1×10^{-3}, which is a higher value than what has been measured in [7]. The submodule capacitances used in (3) have a normal distribution with mean C and variance 1×10^{-4}. The communication from the central controller to all the submodules is disabled from 0.5 to 1 s. Also, at 0.8 s, $\hat{e}_1$ in Table I is decreased to 90 % of its nominal value.

The simulation results of the existing control methods are shown in Fig. 6. The ac-side current i_s (blue) and the current error e (dark red) are given for only M1 used [2] and M1 & M2 used [7] cases. The employed control modes are color-coded on the top lines of the figures. If only M1 is used, the long loss of wireless packets causes overcurrents on the ac and dc-sides and overvoltages in the submodules. When M2 is used in the packet loss period, the MMC performs close to the pre-packet loss period until $\hat{e}_1$ decreases at 0.8 s. Then overcurrents and overvoltages result in. The simulation results of the proposed control methods are shown in Fig. 7. In the figure, $i_d^\star$, i_d, $i_q^\star$ and i_q are the ac-side synchronous frame reference and measured currents, $i_c^\star$ is the reference circulating current, respectively. The M3-rd tag shows the $i_s^\star$ ramp-down period in M3. During M2, the submodules are able to keep i_s close to $i_s^\star$ and minimize e. In M3, they switch to the local closed-loop control and i_s is ramped down to zero smoothly. Thanks to the closed-loop control, the submodules respond quickly to the decrease of $\hat{e}_1$ and avoid overcurrents. When the wireless communication is recovered at 1 s, i_s converges smoothly to $i_s^\star$. Due to lack of carrier synchronization and small but non-zero arm currents, $v_{cu/l}^i$ diverge slightly (up to 10 %) from their nominal value. They converge back to the nominal value when the communication is recovered (not shown in the figure). The simulation results verify the viability of the autonomous operation of submodules with closed-loop current control. The MMC is able to overcome the long packet loss period by using the proposed control methods and mode transitions.

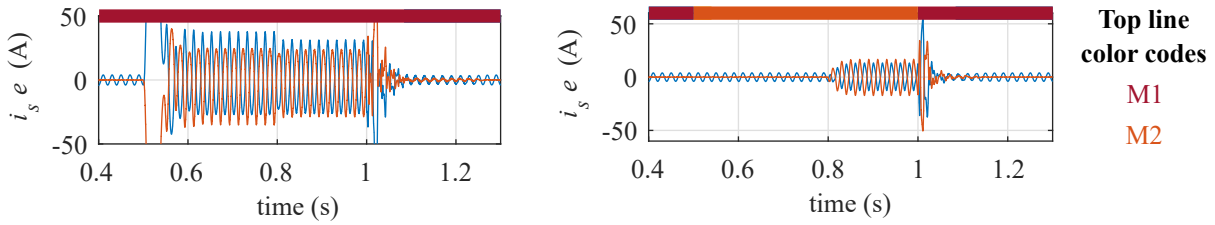

Fig. 6: Simulation results of the existing control methods: left M1 [1, 2], right M1 and M2 [7]. From 0.5 to 1 s, all the submodules do not receive any wireless data; out of this interval, they receive wireless data with the regular packet error rate.

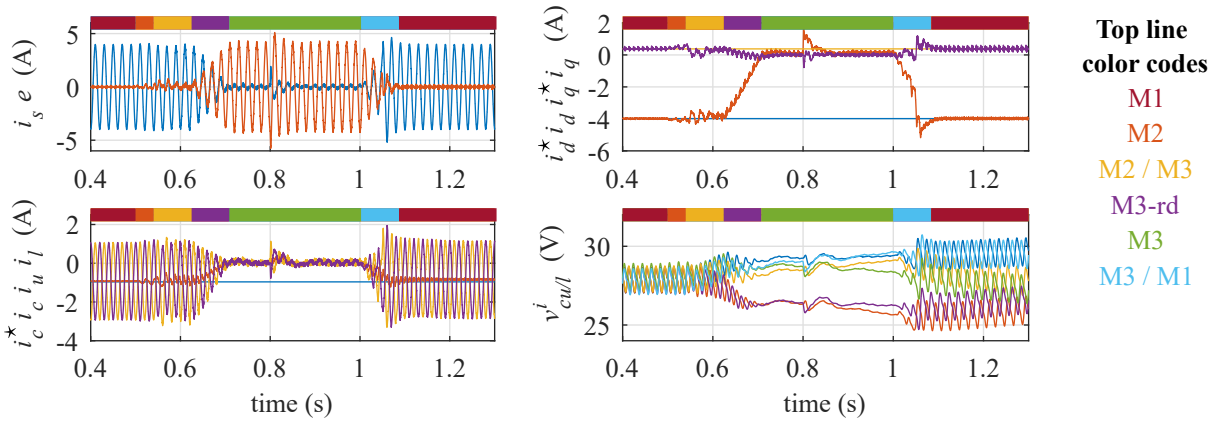

Fig. 7: Simulation results of the proposed control method with autonomous submodules. From 0.5 to 1 s, all the submodules do not receive any wireless data; out of this interval, they receive wireless data with the regular packet error rate.

Experimental Study and Discussion

The experimental study circuit diagram is shown in Fig. 3, left. The MMC central and submodule controllers hardware, wireless transceivers, the connections between those, and the employed wireless communication parameters are the same as in [2]. i_u, i_l, and v_a are fed back to the central controller via wired communication. V_{dc} is fixed as a constant in the central controller. The central controller is 12 meters away from the submodules in a power electronics laboratory, and the wireless transceivers are

in a line of sight. The experiment is conducted in a stationary environment. The packet loss rate in the regular operation is measured previously in the same environment as 7×10^{-4} [7].

The submodules used in the experiments do not have current sensors onboard. Also, the submodule capacitor voltage measurements have too low precision to obtain the arm current from (3). For this reason, as a special case of the experimental setup, the ac-side current transmitted from the central controller is used in the local current controllers in the submodules during M3. That means, practically, the wireless communication between the central controller and the submodules remains all the time. However, the submodules experience a *virtual packet loss period* initiated in all the submodules by a signal transmitted from the central controller. Only the ac-side current data transmitted from the central controller are utilized in the submodules during the virtual packet loss period.

The steady-state (M1) ac-side voltage, ac-side current, arm currents, circulating current, and one submodule capacitor voltage waveforms of the MMC are shown in Fig. 8. The MMC operates stably. Ac-side current and one submodule capacitor voltage waveforms during the virtual packet loss period are shown in Fig. 9. The operational modes that the submodules run in are shown on the top edges of the figures. The virtual packet loss period starts at 0.293 s, and the submodules switch to M2 after two control cycles. In M2, the voltage and current waveforms remain similar to the pre-packet-loss interval. The current amplitude transiently increase up to 70 % during the transition from M2 to M3. It is important to note that, without the transition period, the increase is higher. The M3 operation follows the transition, and $i_s^\star$ is ramped down to zero during M3-rd. Then, M3 continues 92 ms with $i_s^\star$ being zero. At 0.592 s, the virtual packet loss ends, and the transition from M3 to M1 starts. During the transition, current and voltage waveforms experience a transient increase. The MMC operates stably similar to the pre-packet-loss interval when the control is back to M1.

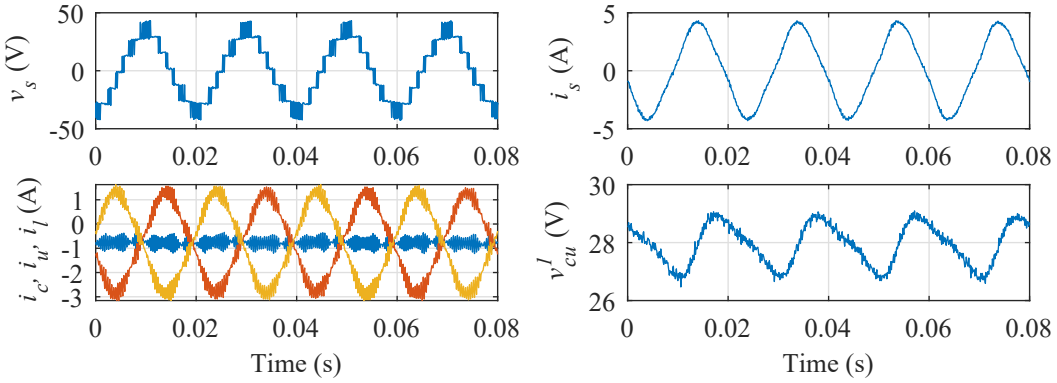

Fig. 8: Experimental results of the steady-state (M1) operation of the MMC with wirelessly controlled submodules. The phase-shift between v_s and i_s is due to taking the measurements at different instances.

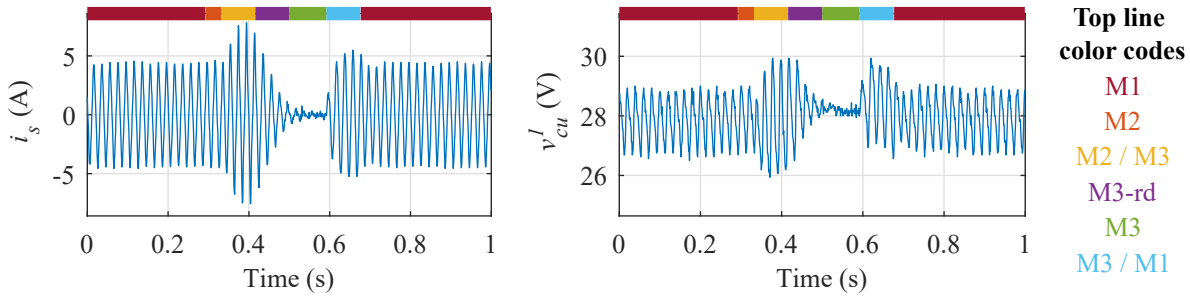

Fig. 9: Experimental results of the autonomous operation of submodules. In M1, submodules receive wireless data with the regular packet error rate. In M2 and M3, submodules do not receive any data.

The experimental results confirm the functionality of the proposed autonomous control of MMC submodules for long wireless packet loss periods. Using the open-loop control (M2), the submodules can continue their modulation with the same pattern prior to the packet loss interval, and with the local-closed

loop controller (M3), they can actively generate their insertion index. Then M3 can drive the submodules to a safe state as in the experiments or continue the modulation with the same current reference prior to the packet loss train until the submodule state variables reach the safety limits. The proposed autonomous control of the submodules does not bring any drawback to the regular operation of the submodules with wirelessly received data.

Conclusion

Wireless control of MMC submodules is an emerging research topic that might present advantages in terms of the cost and availability of the converter. The previously proposed wireless control methods cannot cope with the long wireless packet loss intervals or when the MMC experiences a disturbance on the ac-side in these intervals. Overcurrents and overvoltages in the MMC result in these cases. In this paper, the submodules are proposed to have their own ac-side current controllers to use during the long packet loss intervals. The local controllers in the submodules are replicas of the ac-side current controller in the central controller, and they operate with the locally measured or calculated ac-side current and with the extrapolated current reference from the previous control cycles. The simulation and experimental results have shown that the MMC can safely overcome the long loss intervals thanks to the local closed-loop current control. Consequently, the packet losses do not present a safety concern for the wireless control of MMC submodules.

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