Wireless control of modular multilevel converter submodules under ac-side faults

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Keywords

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Abstract

Wireless control of modular multilevel converter (MMC) submodules has been offered recently with potentially lower cost and higher availability advantages for the converter station. In this paper, the wireless control of MMC submodules under ac-side faults is investigated. The central controller of the MMC is equipped for the unbalanced grid conditions. Local current controllers in the submodules are operated autonomously in case of loss of wireless communication during the fault. A set of simulations with single line-to-ground, line-to-line, and three-phase-to-ground faults reveal that the MMC rides through the faults in all the cases with the expected communication conditions or when the communication is lost before or after the fault instant.

Introduction

The modular multilevel converter (MMC) has been in use in high-voltage multi-megawatt applications, such as high-voltage dc (HVDC) transmission, for more than ten years [1]. Recently, the wireless control of MMC submodules has been proposed [2], implemented, and verified [3]. The distributed control method [4], consisting of a central controller and submodule controllers all with wireless transmission capability, forms the basis of the wireless control proposal. The acclaimed advantages of wireless control of submodules include less material and workforce use for the communication system installation between the controller(s) and submodules leading to cheaper MMC stations, shorter installation time, and higher availability of the MMC station [3]. On the other hand, wireless control brings communication errors and higher latency to the control system compared to the wired control, which can deteriorate the performance of the MMC or even cause destabilization if not minimized and compensated. The total delay is minimized by coordinating the control and communication subsystems and broadcasting the control data [3]. The communication errors are treated by decreasing the closed-loop system control bandwidth [3], extrapolating the previously received data in the submodules [5], and employing individual current controllers in the submodules [6].

Control of voltage-source converters (VSCs) and MMCs under ac-side faults have been studied thoroughly [7, 8, 9, 10]. However, to the best knowledge of the authors, there is no study so far on the control of MMCs consisting of wirelessly controlled submodules under ac-side fault conditions. Handling of ac-side faults while experiencing higher latency, wireless communication errors, and, even worse, a complete loss of communication during the fault might result in complicated dynamics to control.

This paper investigates the feasibility of the wireless control of MMC submodules considering ac-side faults. The positive- and negative-sequence current control, the well-known VSC control method under

unbalanced grid conditions, is applied to the wireless control method used in [3]. Three ac-side fault scenarios are examined with simulation studies while exploiting the treatments proposed in [5, 6] against the wireless communication errors. The simulation studies show that the MMC rides through the ac-side faults with the proposed control system even with complete loss of wireless communication before or after the fault starts.

MMC Control Under Ac-side Faults

In this section, firstly, the general VSC control strategy under ac-side faults is recovered, which applies to the MMCs. Then the control of MMCs under ac-side faults with wirelessly controlled submodules is discussed.

VSC control under ac-side faults

The possible types of ac-side faults in three-phase VSCs can be listed as [11]:

1. single line-to-ground (SLG) fault,
2. line-to-line (LL) fault,
3. double line-to-ground (LLG) fault,
4. three-phase (LLL) fault,
5. three-phase-to-ground (LLLG) fault.

In LLL and LLLG faults, all the phases are affected by the fault equally, assuming they have the same fault resistance. These two *symmetrical* fault types result in balanced ac-side voltages, which are purely positive-sequence. In this case, the positive-sequence current control is sufficient in the VSC. For the first three *asymmetrical* fault types, on the other hand, the phases are affected unequally from the fault, which results in unbalanced ac-side voltages. The unbalanced voltages compose of negative- and zero-sequence components in addition to the positive sequence. The resultant voltage components can drive negative- and zero-sequence current components that can cause overvoltages and overcurrents in the VSC if uncontrolled. If the conventional vector control based on instantaneous power theory is employed [10], then the positive-sequence current control is also distorted as the measured ac-side voltages and currents are not purely positive-sequence anymore. Then, one of the fundamental goals of VSC control under unbalanced grid conditions is to prevent overcurrents, overvoltages and keep control over positive-sequence current. Moreover, the ac grid codes in countries with high wind-power penetration rates require the HVDC stations (mostly MMCs) to inject positive- and negative-sequence reactive currents during the faults to support the voltage recovery [12].

All these goals require independent control of positive-, negative-, and zero-sequence components of the VSC ac-side currents under unbalanced grid conditions with the following exception: if the VSC is connected to the ac grid with a delta/star transformer and delta is on the VSC side, zero-sequence currents are blocked on the VSC side. Then, the zero-sequence current control is not necessary. In this paper, zero-sequence current control is not considered.

The first task to realize the proper control of positive- and negative-sequence currents is to extract the respective sequences of ac-side voltages and synchronize the VSC with the positive-sequence voltage of the ac grid. Two main extraction techniques are presented in the literature: decoupled double synchronous reference frame (DDSRF) [13] and double second-order generalized integrator (DSOGI) [14]. In this paper, the DSOGI extraction technique is preferred since DDSRF is problematic for the VSC passivity due to the filtering in the algorithm [15]. Once the positive-sequence voltage is extracted with DSOGI, it can be used in the conventional synchronous reference frame phase-locked loop without an input filter to synchronize the VSC with the ac grid [16].

In this paper, the positive and negative sequence current references for a three-phase VSC are determined according to the active power reference P and mixed positive- and negative-sequence reactive current injection strategy [10], based on flexible positive/negative sequence control [12]. The current references are defined as

$$i^{\star}_{d^{+1}} = \frac{2}{3}\frac{P}{v_{d^{+1}}}, \qquad i^{\star}_{q^{+1}} = k_{+}(0.9 - V_{+}), \qquad i^{\star}_{d^{-1}} = 0, \qquad i^{\star}_{q^{-1}} = -k_{-}(V_{-} - 0.05). \tag{1}$$

In (1), V_+ and V_- are the positive and negative sequence point of common coupling (PCC) voltages in per unit, v_d^{+1} is the PCC voltage positive sequence d-axis component, k_+ and k_- are the positive and negative sequence droop factors.

The control of positive- and negative-sequence currents can be realized in the synchronous or stationary reference frames with proportional-integral (PI) or proportional-resonant (PR) controllers. PR controllers have the advantage over the PI that the positive- and negative-sequence current references can be added algebraically in the stationary frame and controlled with a single controller. Stationary frame current control is preferred in this paper. The overall VSC control block diagram is shown in Fig. 1. In the figure, superscript s denotes variables in the stationary frame, v_{abc} is the PCC voltage, i_{abc} is the VSC ac-side current. Feedforward of the PCC voltages v_a^s, anti-windup, and saturation of the reference are included in the ac-side current controller block.

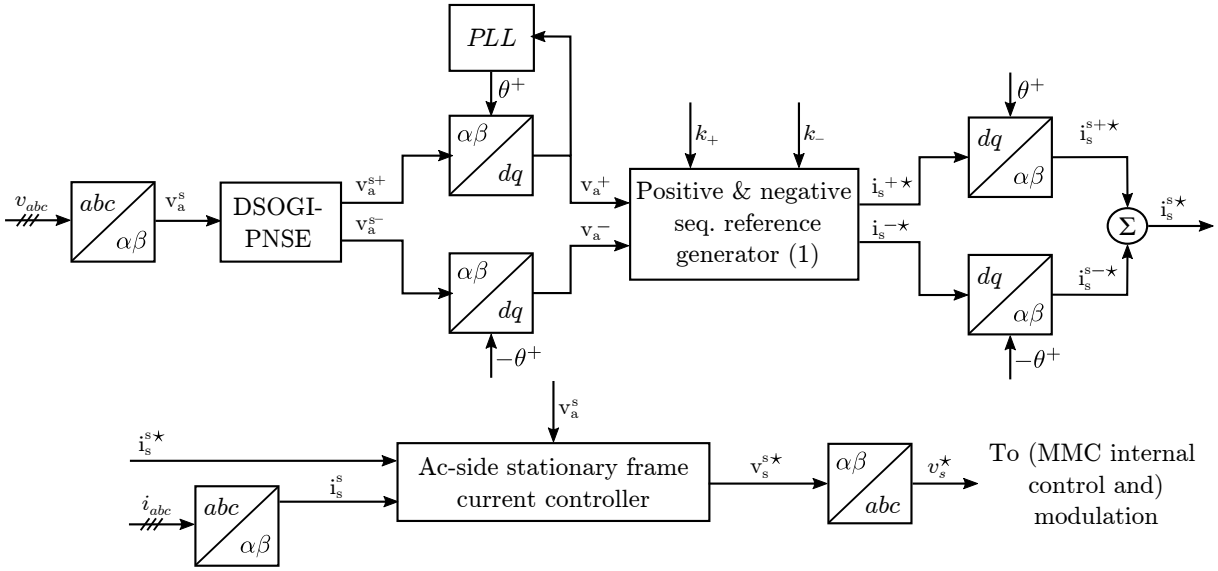

Fig. 1: Block diagram of DSOGI-PNSE-based vector ac-side-current control.

Wireless control of MMC submodules under ac-side faults

The wireless control of MMC submodules has been proposed previously [2]. The basis of the proposal is to have a central controller and submodule controllers with wireless transmission capability, run the ac-side current, circulating current, and arm balancing controls in the central controller, modulation and submodule capacitor voltage control in the submodule controllers, i.e., to implement distributed control [4] with wireless communication. Then, the fundamental data to transmit wirelessly from the central controller to the submodules are the insertion indices and synchronization signal for the modulation carriers. The reader is referred to [3] for further details on the design and verification of the proposal.

The VSC control method under ac-side faults defined in the previous subsection is independent of the MMC-specific control tasks and modulation. Compared to the converter control tasks given in [3], the only change is in the ac-side current control using the same measurements, i.e., ac-side currents and PCC voltages. This change has no practical effect on the proposed wireless control strategy as it is confined to the central controller. Hence, the control method defined in the previous subsection and illustrated in Fig. 1 can be used *as-is* for the wireless control of MMC submodules with no need to modify any other part of the wireless control strategy in [3]. Consequently, the transfer functions of the MMC ac-side current PR controller and open-loop transfer function are obtained, respectively, as

$$F(s) = K_p + \frac{K_1(s\cos\phi_1 - \omega_1\sin\phi_1)}{s^2+\omega_1^2}, \qquad G(s) = F(s)\frac{2}{sL+R}e^{-sT_d}, \tag{2}$$

where s is the complex Laplace variable, K_p is the proportional gain, K_1 is the resonant gain, ϕ_1 is the compensation angle for the total time delay, ω_1 is the fundamental angular frequency, L is the arm

inductance, R is the arm parasitic resistance, T_d is the total delay (including wireless communication). The bandpass filter transfer function of the PCC voltage feedforward and the ac-side admittance of the MMC are obtained, respectively, as

$$H(s) = \frac{\alpha_f(s\cos\phi_1 - \omega_1\sin\phi_1)}{s^2 + \alpha_f s + \omega_1^2}, \qquad Y(s) = \frac{2(1 - H(s)e^{-sT_d})}{sL + R + 2F(s)e^{-sT_d}}, \tag{3}$$

where α_f is the bandwidth of the bandpass filter [15].

It is well known that wireless communication might result in higher latency and data packet losses compared to a properly designed wired communication. The effects of the latency and packet losses and the measures to minimize their effects are discussed previously [3, 5, 6]. With the proposed wireless control method in [3], the randomness in the data latency is minimized. The short data packet losses of up to hundreds of control cycles are treated by extrapolating the received insertion indices in [5]. In case of longer packet losses, the submodules are proposed to ramp the ac-side currents down to zero by their local ac-side current controllers in [6]. The three operational modes proposed for the submodules in [6] are followed in this paper for the wireless control under ac-side faults. The summary of modes is as follows:

1. Mode 1 (M1): As long as the submodule receives wireless data from the central controller, it conducts the modulation and submodule capacitor voltage control based on the received insertion indices.
2. Mode 2 (M2): If the submodule experiences two-cycle or longer packet losses (loss train), the submodule extrapolates the previously received insertion index and continues modulation unless the loss train is longer than a predefined safe-operation interval or the measured/estimated local variables, e.g., submodule capacitor voltage, exceed the safety limits.
3. Mode 3 (M3): In case of excessive loss trains longer than the predefined interval for M2, or if any of the measured/estimated local variables exceeds the safety limits during M2, the submodule switches to the autonomous operation and runs with the local current controller.

An ac-side fault may occur in any of these modes. If it occurs in M1, the MMC central controller can respond to the fault with the DSOGI-PNSE-based ac-side-current control. If it occurs in M2, as soon as the measured/estimated local variables exceed the safety limits as a result of the fault, the submodules should switch to M3 and ramp the ac-side current down to zero with their local ac-side current controllers. The same applies if the fault occurs in M3. Obviously, by ramping the ac-side current to zero, the MMC will not be able to provide reactive power. However, there is no well-defined way yet for the submodules to provide reactive power during this period with access only to the local variables and not to the PCC voltage. In that case, the priority of the control system is considered to be the safety of the components and to avoid overcurrents and overvoltages in the MMC as a result of the fault.

Simulation of MMC with Wirelessly Controlled Submodules Under Ac-side Faults

A set of simulations are conducted in MATLAB Simulink to evaluate the feasibility of wireless control of MMC submodules under ac-side faults. The simulated MMC consists of half-bridge submodules that are modeled with switching devices. The MMC operates in inverter mode connected to the ac grid over a delta/star transformer, delta winding on the MMC side. The neutral point of the star winding is directly grounded. The simulated circuit diagram is shown in Fig. 2.

In the central controller, the DSOGI-PNSE-based vector ac-side current control and circulating current control for the second and fourth harmonic in the stationary reference frame are employed. Direct voltage control (direct modulation) is used for the arm-balancing control. In the simulations, the communication parameters between the central controller and the submodule controllers are tuned to mimic the wireless communication characteristics. The simulation parameters are given in Table I. The packet loss rate given in the table (which is taken roughly five times higher than what has been measured in [5]) is implemented by independent random packet losses for all the communication links between the central

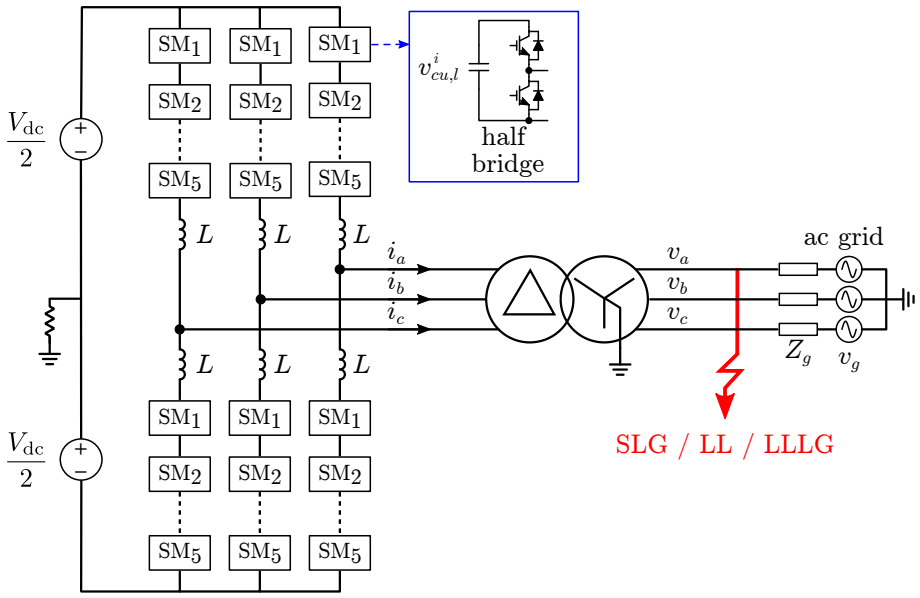

Fig. 2: The simulated circuit diagram. The midpoint of the MMC dc-side is grounded with a high resistance.

controller and the submodules. In the submodules, local ac-side current controllers are installed. During the wireless packet loss periods, the ac-side current is calculated according to the submodule capacitor charge/discharge dynamics in the submodules. The reader is referred to [6] for the details of local controllers in the submodules.

Ac-side current closed-loop system stability and ac-side admittance resulting from the central controller are investigated in Fig. 3 left. In the figure, $G_{cc}(s)$ and $Y_{cc}(s)$ are the open-loop transfer function and ac-side admittance for the central controller. The ac-side current closed-loop system is stable with an 80° phase margin for the central controller. The conductance of $Y_{cc}(j\omega)$ goes slightly down to the negative region around ω_1 and after $20\omega_1$. The analyses are repeated for the submodule controllers in Fig. 3 right, where $G_{sc}(s)$ and $Y_{sc}(s)$ are the open-loop transfer function and ac-side admittance for the submodule controllers. The ac-side current closed-loop system is stable with a 72° phase margin for the submodule controllers. The conductance of $Y_{sc}(j\omega)$ goes slightly down to the negative region around ω_1.

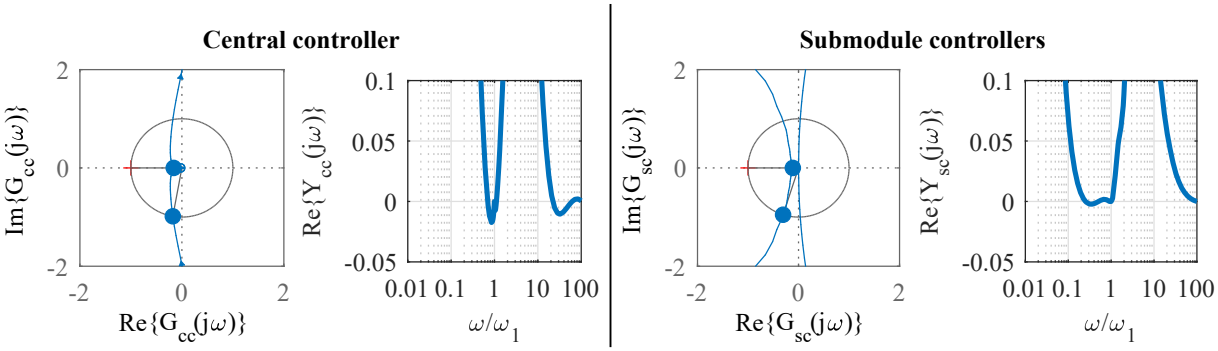

Fig. 3: Nyquist plot of the ac-side current open-loop transfer function and the real part of the MMC ac-side admittance for the central controller (left) and submodule controllers (right).

Three fault types are investigated with the three fault scenarios: Control of the MMC with an SLG, LL, or LLLG fault on the grid side of the transformer with

1. the expected wireless packet loss and delay characteristics given in Table I,
2. conditions in scenario 1 and a wireless packet loss train that starts after the fault instant,
3. conditions in scenario 1 and a wireless packet loss train that starts before the fault instant.

The first scenario corresponds to when the fault occurs in the normal operating conditions of wirelessly

Table I: Simulation parameters

	Symbol	Value		Symbol	Value
Fundamental frequency	ω_1	$2\pi 50$ rad/s	Switching frequency	f_c	833 Hz
Submodules per arm	N	5	Dc-side voltage	V_{dc}	200 V
Ac-grid peak voltage	$\hat{v}_g$	94 V	Arm inductance	L	3 mH
Arm parasitic resistance	R	0.3 Ω	Submodule capac.	C	2.7 mF
Active power reference	P	1.5 kW	Reactive power ref.	Q	0 var
Sampling frequency				ω_s	$2\pi 10$ krad/s
Ac-side-current closed-loop-system bandwidth in the central controller				α_c	$\omega_s/60$ [rad/s]
Ac-side-current resonant bandwidth in the central controller				α_1	$\alpha_c/100$ [rad/s]
Ac-side-current closed-loop-system bandwidth in the submodule cont.				α_{cs}	$\omega_s/20$ [rad/s]
Ac-side-current resonant bandwidth in the submodule controllers				$\alpha_{1\mathrm{s}}$	$\alpha_{\mathrm{cs}}/10$ [rad/s]
Ac-side-current controller proportional gain				$K_{\mathrm{p(s)}}$	$\alpha_{\mathrm{c(s)}}L/2$ [Ω]
Ac-side-current controller resonant gain				$K_{1(\mathrm{s})}$	$\alpha_{\mathrm{c(s)}}\alpha_{1(\mathrm{s})}L$ [Ω/s]
PCC voltage bandpass filter bandwidth in the central controller				α_f	1000 rad/s
PCC voltage bandpass filter bandwidth in the submodule controllers				α_{fs}	0 rad/s
Total time delay for the central controller [3]				T_d	242 μs
Total time delay for submodule controllers [3]				T_{ds}	50 μs
Packet loss rate for wireless communication [5]				-	1×10^{-3}
Positive and negative sequence droop factors				k_+, k_-	2.5

controlled submodules. The normal conditions refer to a predefined ratio of random packet losses and a fixed time delay, as given in Table I. The submodules should operate in M1 operation mode in this scenario. In the second scenario, the submodules should be in M1 operation mode before the loss train starts, and they should switch to M2 and M3 modes sequentially after the loss train. In the third scenario, firstly, the communication is lost in all the submodules, and then the fault occurs. The submodules might be in M2 or M3 mode, depending on when the fault happens after the loss of communication. Since the fault occurs after the loss of communication, the submodules should ride through the fault autonomously. The performances of the three scenarios are benchmarked with a reference scenario (tagged as R) which mimics the wired communication conditions, i.e., no packet loss, fully synchronized modulation carriers, and only pulse-width modulation delay, which is equal to the total time delay for submodule controllers.

Simulation results and discussion

The simulation results are shown in Figs. 4-6 for the SLG, LL, and LLLG faults, respectively. In all the figures, for each simulation scenario, the following waveforms are shown from top to bottom: (a) PCC voltage, v_{abc}, (b) MMC ac-side currents i_{abc}, and circulating currents, $i_{\mathrm{c,abc}}$, (c) synchronous frame d-axis positive and negative sequence reference and measured currents, $i_d^{+\star}, i_d^{+}, i_d^{-\star}, i_d^{-}$, (d) synchronous frame q-axis positive and negative sequence reference and measured currents, $i_q^{+\star}, i_q^{+}, i_q^{-\star}, i_q^{-}$, and (e) capacitor voltages of phase a, $v_{c,a}^{i}$. In all the scenarios, the fault starts at 0.58 s and continues until 0.68 s. In scenarios 2, the complete loss of communication happens between 0.63 and 0.78 s. In scenarios 3, the complete loss of communication happens between 0.48 and 0.78 s. The response of the MMC for different faults is similar. When scenarios R and 1 are compared in each figure, wireless communication has no visible effect on the waveforms except marginally higher spread of capacitor voltages. In scenarios 2, while the MMC follows the current references until the loss of communication, after that instant, the submodules switch to M3 operation mode and drive the ac-side current to zero as planned. In scenarios 3, the faults start when the submodules are already in operation mode M3. The submodules keep the ac-side and circulating currents at zero throughout the fault and until the communication is recovered. Then they switch back to M1. In scenarios 2 and 3, during the loss of communication, the submodule capacitor voltages diverge from their nominal value due to the loss of synchronization signal for the modulation carriers, resulting in errors in the phase of the carriers [2]. It is hypothesized that a self-synchronization algorithm embedded in the submodules can (partially) correct the phases and suppress the voltage spread.

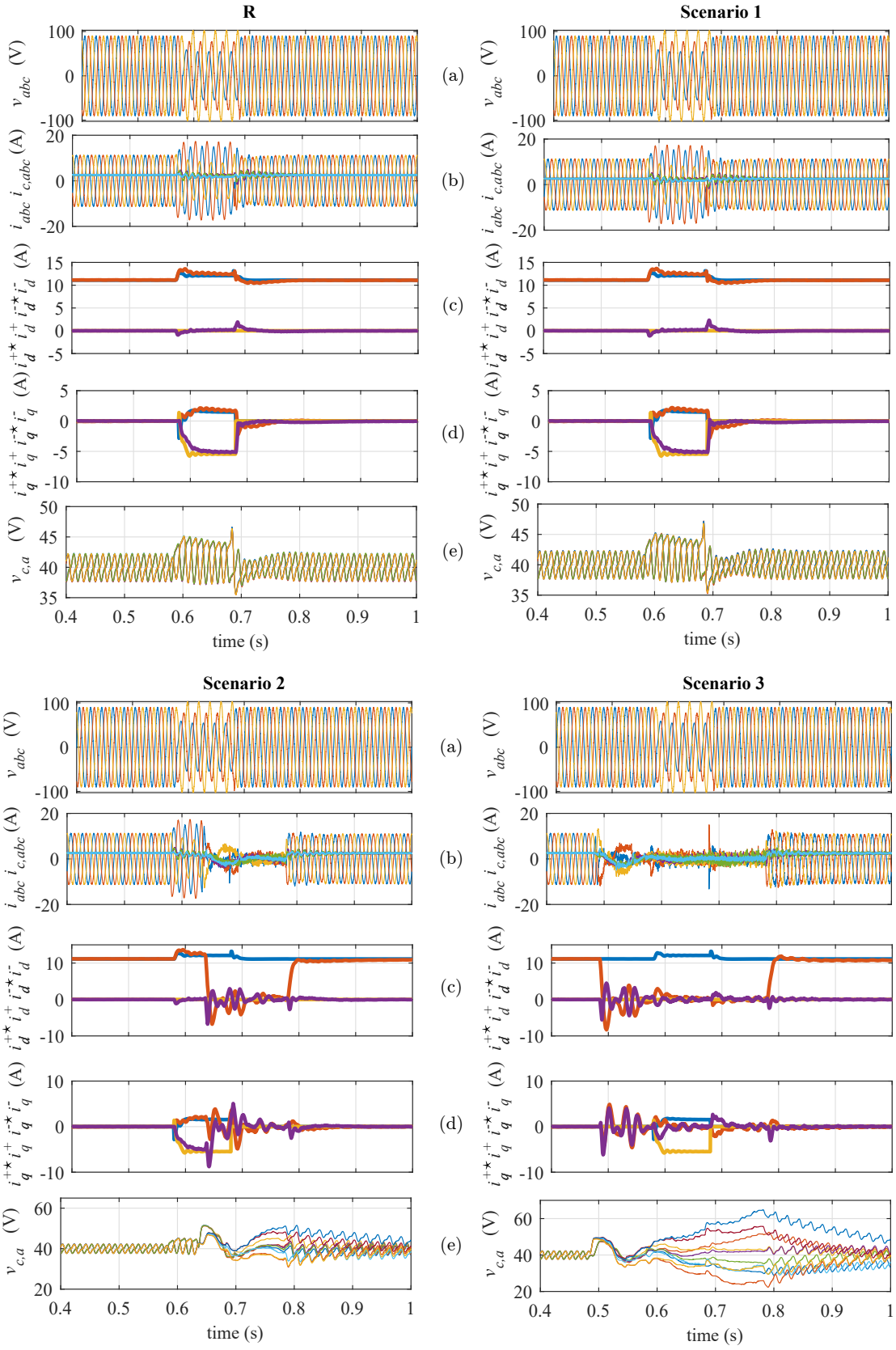

Fig. 4: SLG fault simulation results with communication characteristics corresponding to the ideal case with no packet loss and only modulation delay (R), with random packet losses with the predefined loss rate and time delay (Scenario 1), characteristics in Scenario 1 and a complete loss of communication between 0.63 and 0.78 s (Scenario 2), characteristics in Scenario 1 and a complete loss of communication between 0.48 and 0.78 s (Scenario 3). In all the cases, the SLG fault happens from 0.58 to 0.68 s.

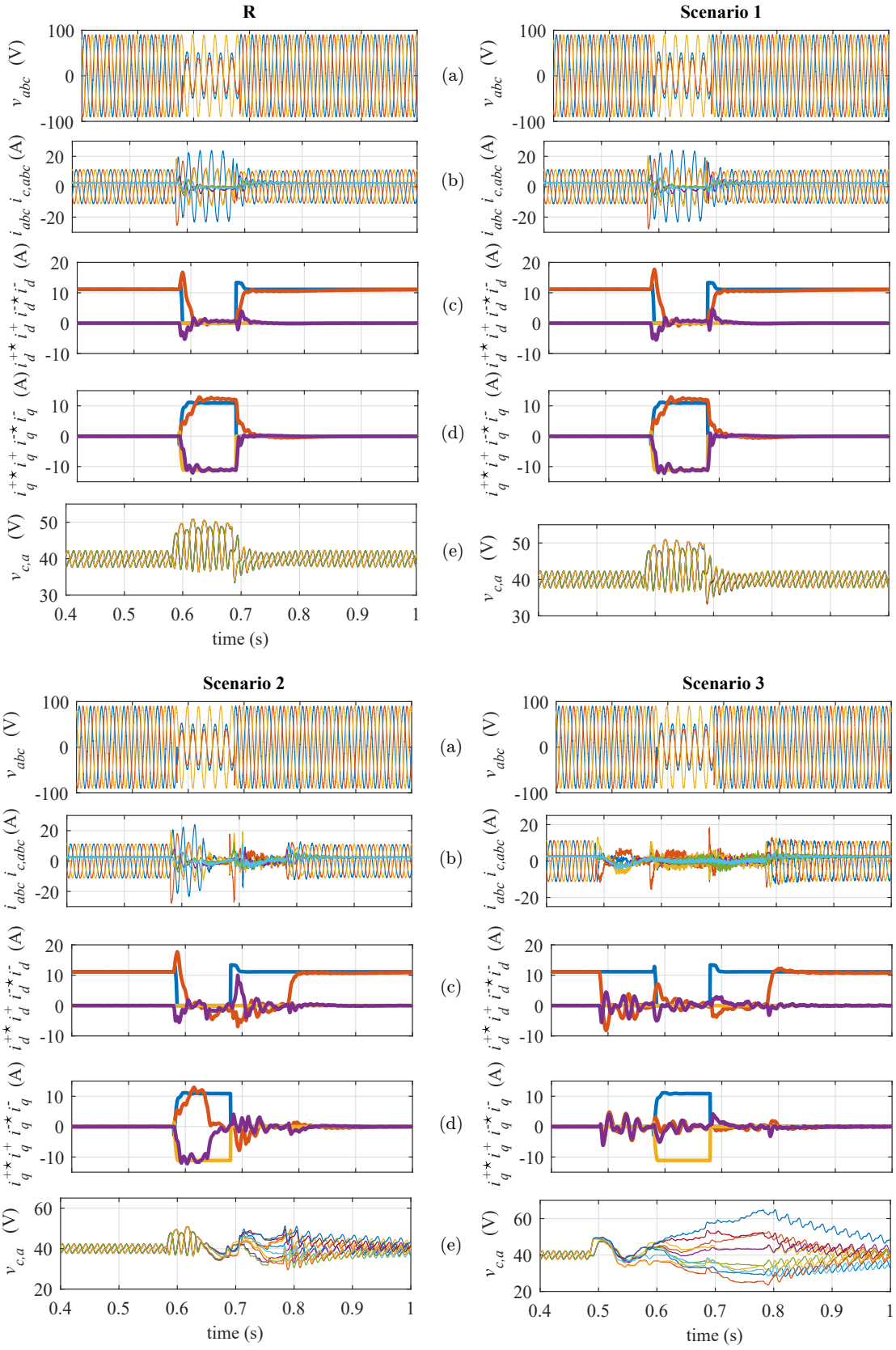

Fig. 5: LL fault simulation results with communication characteristics corresponding to the ideal case with no packet loss and only modulation delay (R), with random packet losses with the predefined loss rate and time delay (Scenario 1), characteristics in Scenario 1 and a complete loss of communication between 0.63 and 0.78 s (Scenario 2), characteristics in Scenario 1 and a complete loss of communication between 0.48 and 0.78 s (Scenario 3). In all the cases, the LL fault happens from 0.58 to 0.68 s.

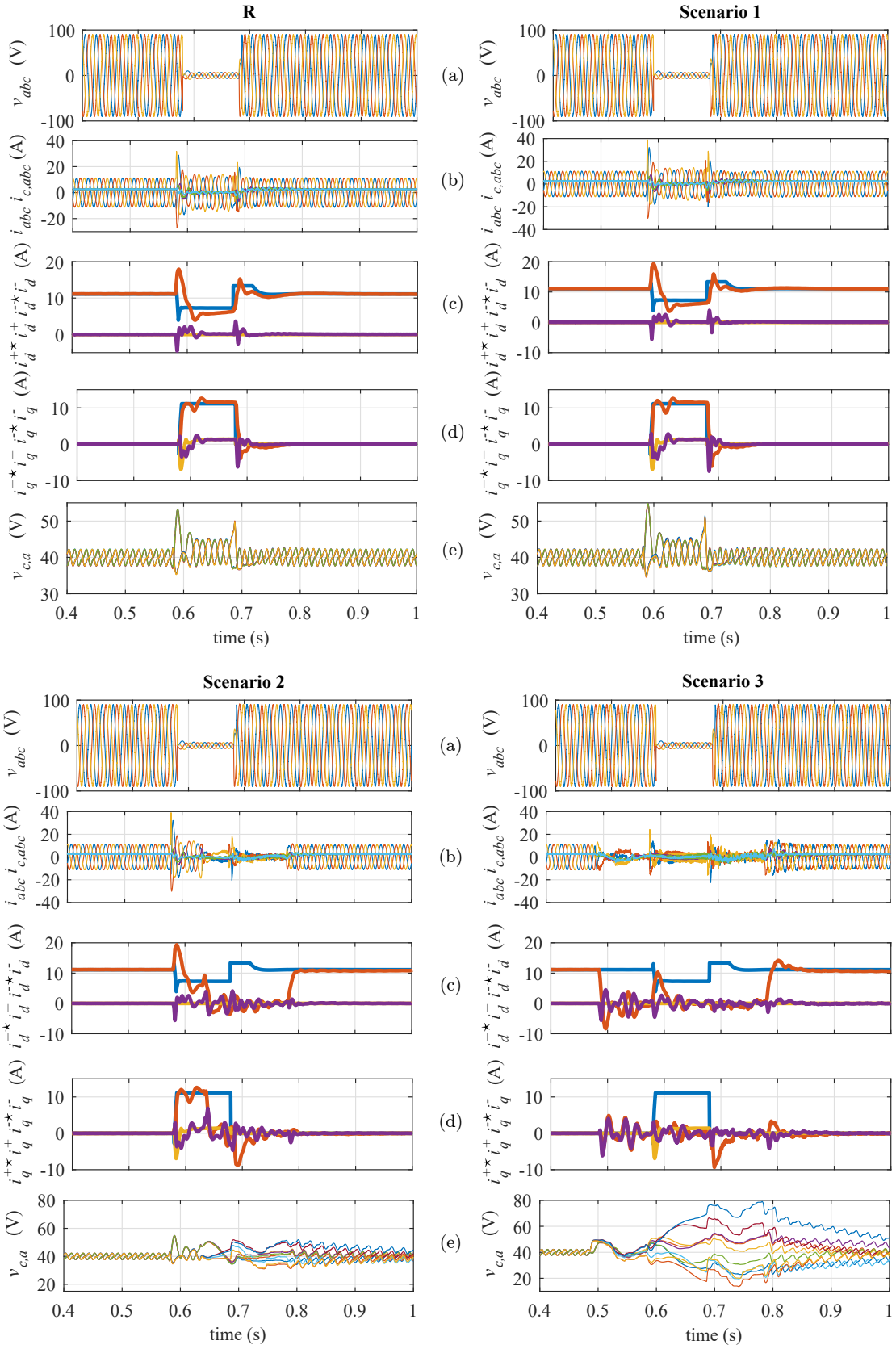

Fig. 6: LLLG fault simulation results with communication characteristics corresponding to the ideal case with no packet loss and only modulation delay (R), with random packet losses with the predefined loss rate and time delay (Scenario 1), characteristics in Scenario 1 and a complete loss of communication between 0.63 and 0.78 s (Scenario 2), characteristics in Scenario 1 and a complete loss of communication between 0.48 and 0.78 s (Scenario 3). In all the cases, the LLLG fault happens from 0.58 to 0.68 s.

The self-synchronization algorithm would be based on the average synchronization period calculated in each submodule when the communication is healthy. The hypothesis is left as a future research subject.

Conclusion

The wireless control of MMC submodules under ac-side faults is investigated in this paper. The well-known VSC control methods under unbalanced grid conditions, like DSOGI-PNSE-based vector ac-side current control, can be applied to the wireless control approach based on distributed control of MMCs. Autonomous controllers in the submodules are used when wireless communication errors and faults happen simultaneously. The simulation results have shown that the MMC rides through the SLG, LL, and LLLG faults even with a complete loss of communication before or after the fault instant by using the proposed control method.

References

[1] Westerweller T., Friedrich K., Armonies U., Orini A., Parquet D., Wehn S.: Trans bay cable–Worlds first HVDC system using multilevel voltage-sourced converter, in Proc. Cigre Session, 2010, pp. 1-6.

[2] Ciftci B., Gross J., Norrga S., Kildehøj L., Nee H.-P.: A proposal for wireless control of submodules in modular multilevel converters, in 20th Eur. Conf. Power Electron. and Appl., Riga, 2018, pp. 1-10.

[3] Ciftci B., Schiessl S., Gross J., Harnefors L., Norrga S., Nee H.-P.: Wireless control of modular multilevel converter submodules, IEEE Trans. Power Electron., vol. 36, no. 7, pp. 8439-8453, Jul. 2021.

[4] Ciftci B., Gross J., Norrga S., Nee H.-P.: Simple distributed control for modular multilevel converters, in 21st Eur. Conf. Power Electron. and Appl., Genova, 2019, pp. 1-10.

[5] Ciftci B., Harnefors L., Wang X., Gross J., Norrga S., Nee H.-P.: Wireless control of modular multilevel converter submodules with communication errors, submitted for publication.

[6] Ciftci B., Harnefors L., Wang X, Gross J., Norrga S., Nee H.-P.: Wireless control of modular multilevel converter autonomous submodules, in 23rd Eur. Conf. Power Electron. and Appl., virtual, 2021, pp. 1-10.

[7] Adam G. P., Ahmed K. H., Finney S. J., Williams B. W.: AC fault ride-through capability of a VSC-HVDC transmission systems, in IEEE Energy Convers. Congr. and Expo., Atlanta, GA, 2010, pp. 3739-3745.

[8] Guan M., Xu Z.: Modeling and control of a modular multilevel converter-based HVDC system under unbalanced grid conditions, IEEE Trans. Power Electron., vol. 27, no. 12, pp. 4858-4867, Dec. 2012.

[9] Shi X., Wang Z., Liu B., Liu Y., Tolbert L. M., Wang F.: Characteristic investigation and control of a modular multilevel converter-based HVDC system under single-line-to-ground fault conditions, IEEE Trans. Power Electron., vol. 30, no. 1, pp. 408-421, Jan. 2015.

[10] Sharifabadi K., Harnefors L., Nee H.-P., Norrga S., Teodorescu R.: Control under unbalanced grid conditions, in Design, Control, and Application of Modular Multilevel Converters for HVDC Transmission Systems. Chichester, UK: Wiley-IEEE Press, 2016, ch. 4, pp. 214-231.

[11] Guide for electromagnetic transient studies involving VSC converters, CIGRE Technical Brochure WG B4.70, 2021.

[12] Teodorescu R., Liserre M., Rodriguez P.: Control of grid converters under grid faults, in Grid Converters for Photovoltaic and Wind Power Systems. IEEE, 2007, ch. 10, pp. 237-287.

[13] Rodriguez P., Pou J., Bergas J., Candela J. I., Burgos R. P., Boroyevich D.: Decoupled double synchronous reference frame PLL for power converters control, IEEE Trans. Power Electron., vol. 22, no. 2, pp. 584-592, Mar. 2007.

[14] Rodriguez P., Luna A., Ciobotaru M., Teodorescu R., Blaabjerg F.: Advanced grid synchronization system for power converters under unbalanced and distorted operating conditions, in 32nd Annu. Conf. IEEE Ind. Electron., Paris, 2006, pp. 5173-5178.

[15] Harnefors L., Yepes A. G., Vidal A., Doval-Gandoy J.: Passivity-based stabilization of resonant current controllers with consideration of time delay, IEEE Trans. Power Electron., vol. 29, no. 12, pp. 6260-6263, Dec. 2014.

[16] Rodriguez P., Teodorescu R., Candela I., Timbus A. V., Liserre M., Blaabjerg F.: New positive-sequence voltage detector for grid synchronization of power converters under faulty grid conditions, in 37th IEEE Power Electron. Specialists Conf., Jeju, 2006, pp. 1-7.